Burst BPSK Modem IP Core Specification

Release Information

Name	Burst BPSK Modem IP Core
Version	2.0
Build date	2017.11
Ordering code	ip-burst-bpsk-modem
Specification revision	r1884

Features

The IP core implements full-featured digital burst BPSK modem and is intended for microwave communication systems operating in half-duplex mode.

License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The Burst BPSK Modem IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the Burst BPSK Modulator IP Core block diagram.

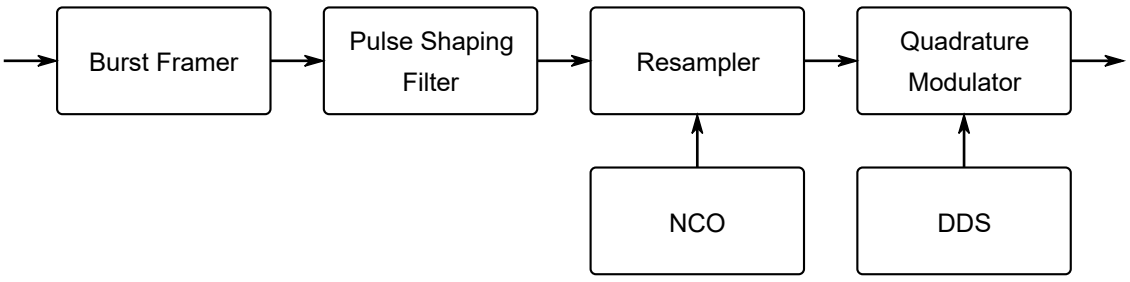

Figure 1. The Burst BPSK Modulator IP Core block diagram

The Burst BPSK Modulator consists of a burst framer and a BPSK modulator.

Figure 2 shows the Burst BPSK Demodulator IP Core block diagram.

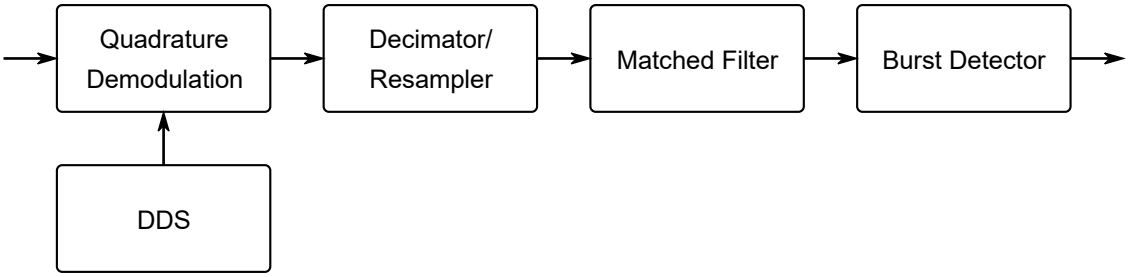

Figure 2. The Burst BPSK Demodulator IP Core block diagram

The Burst BPSK Demodulator consists of a non-coherent BPSK demodulator and a burst detector.

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the Burst BPSK Modulator IP Core.

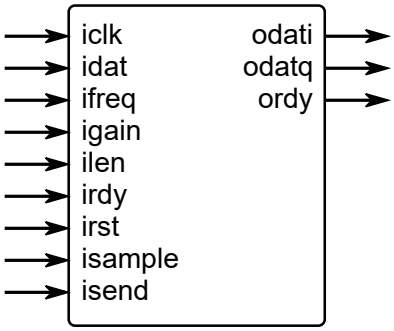

Figure 3. The Burst BPSK Modulator port map

Table 1. The Burst BPSK Modulator port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	1	Input (information) data.
ifreq	32	Output intermediate frequency.
igain	16	Output gain control.
ilen	8	Set useful payload size of a packet. ilen is set in bytes minus 1. For example, ilen=31 means 32 bytes payload.
irdy	1	Modulator output data request.

irst	1	The IP Core synchronously reset when irst is asserted high.
isample	32	Bandwidth control (symbol rate).
isend	1	Burst send command.
odati odatq	W_DAC	Modulator complex IQ output at baseband or at intermediate frequency.
ordy	1	Ready to accept input data.

Figure 4 shows a graphic symbol, and Table 2 describes the ports of the Burst BPSK Demodulator IP Core.

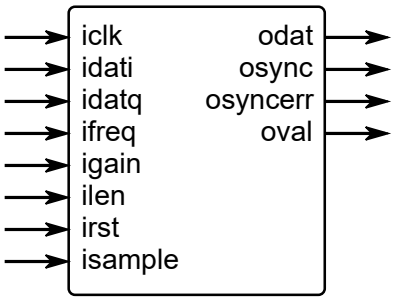

Figure 4. The Burst BPSK Demodulator port map

Table 2. The Burst BPSK Demodulator port map description		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idati idatq	W_ADC	Complex IQ input at baseband or at intermediate frequency.
ifreq	32	Setup input intermediate frequency.
igain	6	CIC Filter gain control in receiver.
ilen	8	Set useful payload size of a packet. ilen is set in bytes minus 1. For example, ilen=31 means 32 bytes payload.
irst	1	The IP Core synchronously reset when irst is asserted high.

isample	32	Bandwidth control (symbol rate).
odat	1	Output (Information) data.
osync	1	Preamble correct acquisition.
osyncerr	1	Error in preamble acquisition.
oval	1	Output data valid signal.

IP Core Operation Description

Key features of the IP Core:

- Burst packet mode
- Synchronous, high-speed algorithm for BPSK signal modulation
- Symbol rate changes 1/4 to 1/16384 of the system clock frequency
- Maximum carrier frequency error between two modems is up to ±12.5% of symbol rate
- Maximum symbol rate error between two modems is up to ±0.5/(8*(ilen+5)) of symbol rate
- Automatic preamble and CRC16 insert and remove
- Fully digital detection and demodulation of the data bursts
- Fixed delay in modulator and demodulator

Figure 5 shows the modem's packet structure. The packet consists of 32 bits preamble, 1-256 bytes payload, 16 bits CRC16. A single bit is equal to a single BPSK symbol.

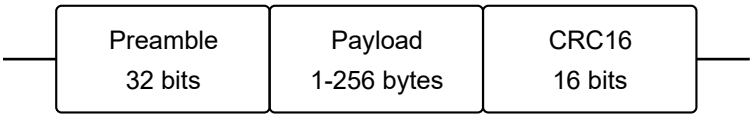

Figure 5. Packet structure

IP Core Parameters

Table 3 describes the Burst BPSK Modem IP Core parameters, which must be set before synthesis.

Table 3. The Burst BPSK Modem IP Core parameters description	
Parameter	Description
W_ADC	**ADC Width**. Width of the Demodulator input samples from ADC (**idati/idatq**).
W_DAC	**DAC Width**. Width of the Modulator output samples to DAC (**odati/odatq**).

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the Burst BPSK Modulator IP Core measurement results.

Table 4. The Burst BPSK Modulator performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_DAC = 16	Altera Cyclone V 5CEFA7			
	555 ALMs (1%) 1 M10K RAM block (1%) 12 DSP (18x18) (8%)	-8, Fmax	-7, Fmax	-6, Fmax
		120.0 MHz 30.0 MSPS to 7.3 KSPS	130.0 MHz 32.5 MSPS to 7.9 KSPS	160.0 MHz 40.0 MSPS to 9.7 KSPS
W_DAC = 16	Xilinx Virtex-7 XC7VX330T			
	288 Slices (1%) 1 18K RAM blocks (1%) 12 DSP (18x18) (2%)	-1, Fmax	-2, Fmax	-3, Fmax
		250.0 MHz 62.5 MSPS to 15.2 KSPS	300.0 MHz 75.0 MSPS to 18.3 KSPS	344.0 MHz 86.0 MSPS to 21.0 KSPS

Table 5 summarizes the Burst BPSK Demodulator IP Core measurement results.

Table 5. The Burst BPSK Demodulator performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_ADC = 14	Altera Cyclone V 5CEFA7			
	3657 ALMs (7%) 5 M10K RAM block (1%) 6 DSP (18x18) (4%)	-8, Fmax	-7, Fmax	-6, Fmax
		104.0 MHz 26.0 MSPS to 6.4 KSPS	120.0 MHz 30.0 MSPS to 7.3 KSPS	146.0 MHz 36.5 MSPS to 8.9 KSPS
W_ADC = 14	Xilinx Virtex-7 XC7VX330T			
	2290 Slices (5%) 1 18K RAM blocks (1%) 6 DSP (18x18) (2%)	-1, Fmax	-2, Fmax	-3, Fmax
		222.0 MHz 55.5 MSPS to 13.5 KSPS	254.0 MHz 63.5 MSPS to 15.5 KSPS	296.0 MHz 74.0 MSPS to 18.0 KSPS

IP Core Interface Description

Figure 6 shows an example of the waveform of the input interface. Handshake port **ordy** controls input dataflow. Input data is read from the input **idat** only when **ordy** is equal to logical one ("1").

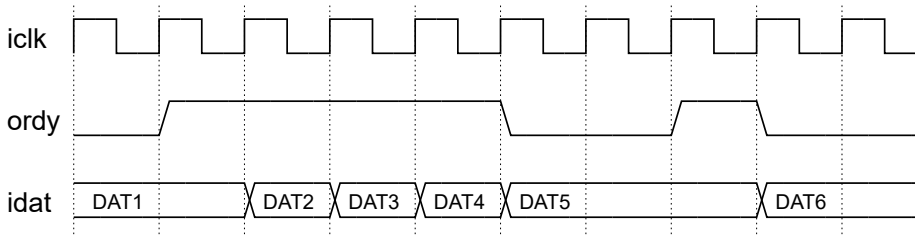

Figure 6. The timing diagrams of the Burst BPSK Modulator operation

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/burst-bpsk-modem/

Feedback

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Revision history

Version	Date	Changes
2.0	2017.11.14	Added support for AD9361, AD9363, AD9364, AD9371, AD9375 and AD9789
1.1	2016.04.06	Added support for payload size 4 to 256 bytes
1.0	2016.03.01	Official release