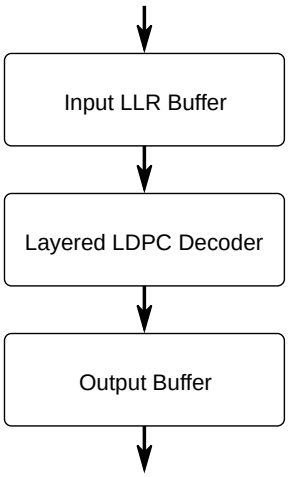
CCSDS AR4JA LDPC Encoder / Decoder IP Core

IP Core Features

- Rate 1/2, 2/3, 4/5
- Block 1K, 4K, 16K
- Up to 90 Mbit/s
- Low implementation loss
- Low FPGA resource usage

Consultative Committee for Space Data Systems



Key Features

- Compliant with CCSDS 131.0-B-4 Standard, April 2022:
  - TM synchronization and channel coding
- Supports all 9 LDPC encoding schemes:
  - Rate = 1/2, (2048, 1024), (8192, 4096), (32768, 16384)
  - Rate = 2/3, (1536, 1024), (6144, 4096), (24576, 16384)
  - Rate = 4/5, (1280, 1024), (5120, 4096), (20480, 16384)
- High throughput architecture:
  - Encoding rate up to 100 Mbit/s
  - Decoding rate up to 90 Mbit/s
- On-the-fly block type change
- Layered Min-Sum-Offset decoding with low implementation loss
- Decoding early termination mechanism
- Variable number of decoding iterations up to 256

Applications

- Satellite communication systems
- Systems with the need of powerful LDPC Codes
- Telemetry (TM) Space Data Link Protocol modems
- Unified Space Data Link Protocol (USLP) modems

Deliverables

- Encrypted Netlist or Complete RTL Source Code versions
- IP Core testbench scripts and design examples for evaluation boards
- Comprehensive integration guide
- Free 1 year technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Royalty-free license without quantitative restrictions
- Off-the-shelf Xilinx and Analog Devices evaluation boards support

IPRIUM