DVB-CID Demodulator IP Core Specification

Release Information

Name	DVB-CID Demodulator IP Core
Version	1.0
Build date	2014.12
Ordering code	ip-dvb-cid-demodulator
Specification revision	r1620

Features

The IP core is full-featured digital DVB-CID demodulator/detector/receiver and is fully compatible with this standard:

- ETSI TS 103 129 v1.1.1 (2013-05)

Price and License

Price:

- Netlist price : 13770 EUR
- Source code price : 73850 EUR
- +10% of the cost for each additional FPGA family netlist
- Customization price is 1000-5000 EUR

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The DVB-CID Demodulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the DVB-CID Demodulator IP Core block diagram.

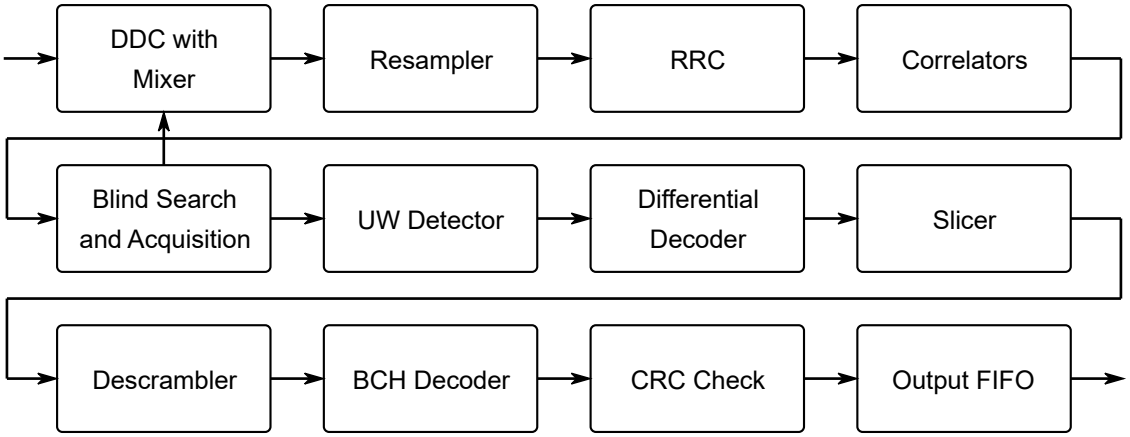

Figure 1. The DVB-CID Demodulator IP Core block diagram

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the DVB-CID Demodulator IP Core.

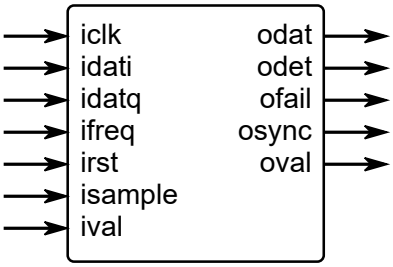

Figure 2. The DVB-CID Demodulator port map

Table 1. The DVB-CID Demodulator port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idati idatq	8	demodulator complex IQ input at baseband or at intermediate frequency
ifreq	32	input intermediate frequency
irst	1	The IP Core synchronously reset when irst is asserted high.
isample	32	DDC sampling rate control
ival	1	input data valid
odat	1	decoded information
odet	1	signal lock detector

ofail	1	decoding fail signal
osync	1	synchronize codewords by syncbyte
oval	1	output data valid

IP Core Parameters

Table 2 describes the DVB-CID Demodulator IP Core parameters, which must be set before synthesis.

Table 2. The DVB-CID Demodulator IP Core parameters description

Parameter	Description
There are no parameters available to change	

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the DVB-CID Demodulator IP Core measurement results.

Table 3. The DVB-CID Demodulator performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
	Altera Cyclone V 5CEFA7			
	36585 ALMs (81%) 351 M10K RAM blocks (51%) 66 DSP (18x18) (43%)	-8, Fmax	-7, Fmax	-6, Fmax
		150.0 MHz	169.0 MHz	193.0 MHz
	Xilinx Virtex-7 XC7VX330T			
	18522 Slices (37%) 270 18K RAM blocks (19%) 66 DSP (18x18) (6%)	-1, Fmax	-2, Fmax	-3, Fmax
		254.0 MHz	310.0 MHz	323.0 MHz

IP Core Interface Description

The IP Core requires additional CPU coprocessor to control signal blind search parameters. Figure 3 shows the connection diagram of the DVB-CID Demodulator IP Core with CPU coprocessor.

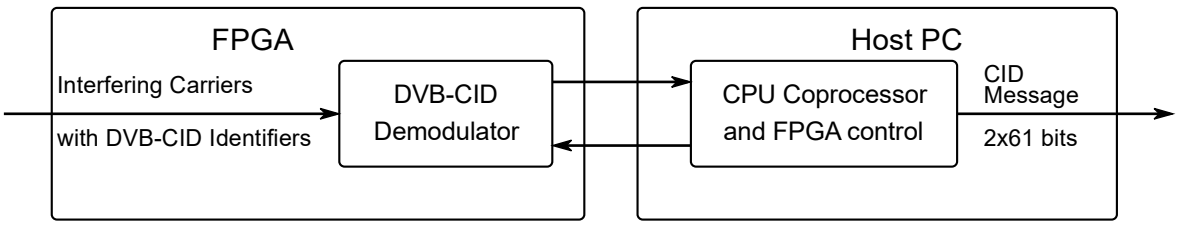

Figure 3. Connection diagram of the IP Core to the CPU coprocessor.

Figure 4 shows an example of the waveform of the input interface.

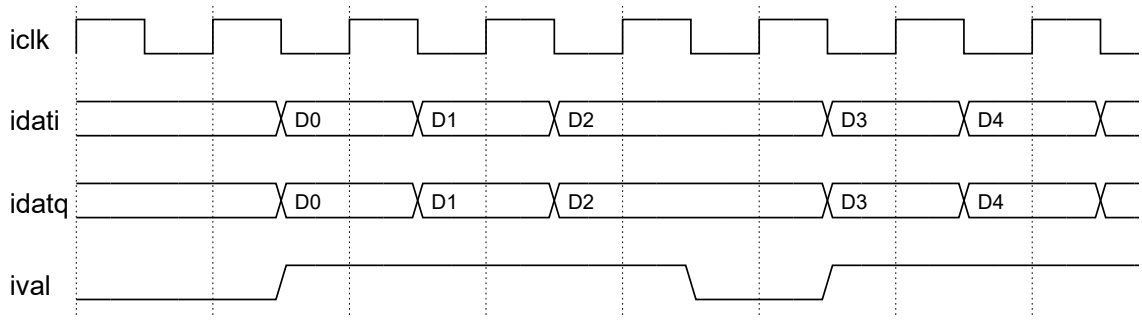

Figure 4. The timing diagram of the IP Core input interface.

Figure 5 shows an example of the waveform of the output interface.

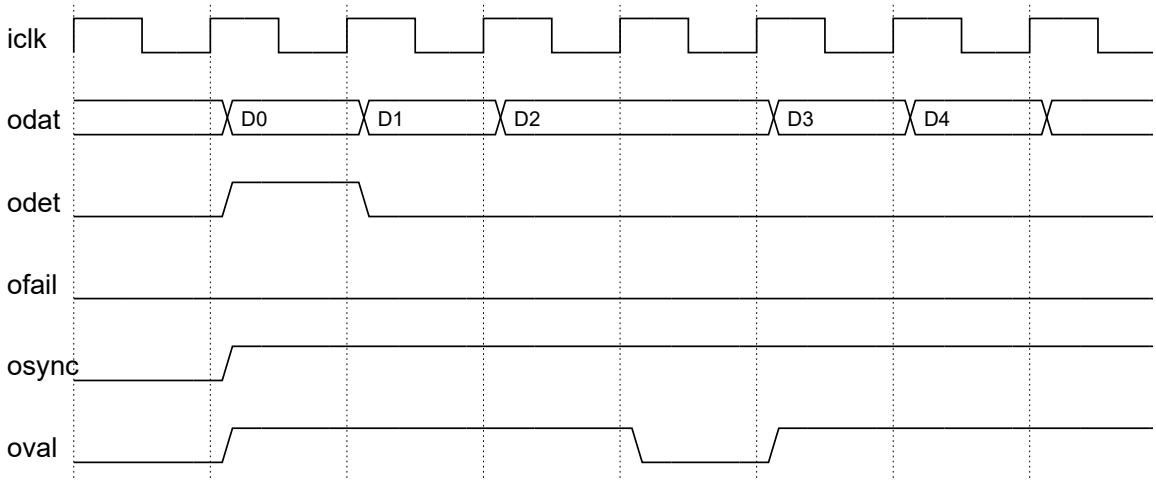

Figure 5. The timing diagram of the IP Core output interface.

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/dvb-cid-demodulator/

Feedback

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Revision history

Version	Date	Changes
1.0	2014.12.02	Official release