



DVB-S2 Modulator IP Core  
Specification

## Release Information

Name	DVB-S2 Modulator IP Core
Version	5.0
Build date	2017.11
Ordering code	ip-dvbs2-modulator
Specification revision	r1383

## Features

The IP core is digital DVB-S2 modulator and is fully compatible with this standard:

- ETSI EN 302 307 (v1.4.1)

## Deliverables

The DVB-S2 Modulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

## IP Core Structure

Figure 1 shows the DVB-S2 Modulator IP Core block diagram.

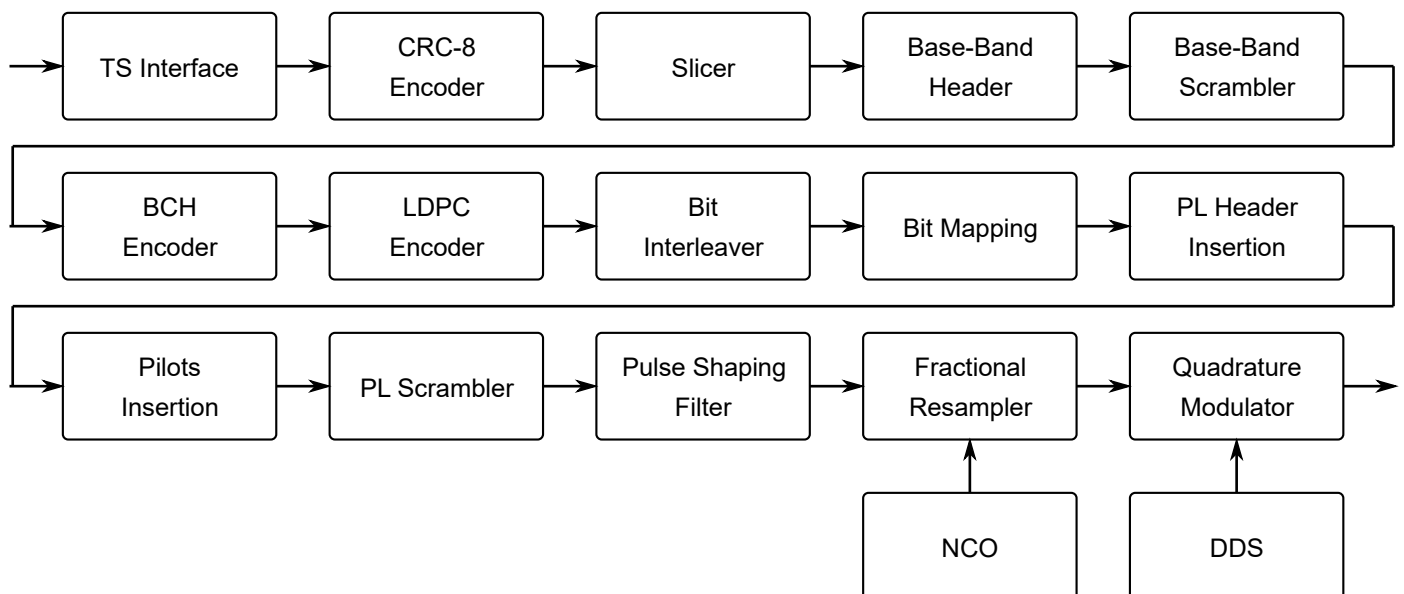


Figure 1. The DVB-S2 Modulator IP Core block diagram

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the DVB-S2 Modulator IP Core.

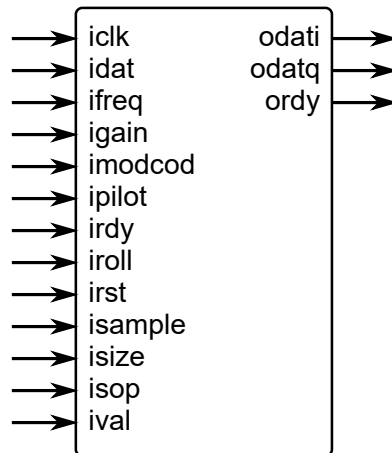


Figure 2. The DVB-S2 Modulator port map

Table 1. The DVB-S2 Modulator port map description		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	8	input (information) data
ifreq	32	output intermediate frequency
igain	16	output gain control

imodcod	5	<p>modulation and coding:</p> <p>1 - QPSK 1/4  2 - QPSK 1/3  3 - QPSK 2/5  4 - QPSK 1/2  5 - QPSK 3/5  6 - QPSK 2/3  7 - QPSK 3/4  8 - QPSK 4/5  9 - QPSK 5/6  10 - QPSK 8/9  11 - QPSK 9/10</p> <p>12 - 8PSK 3/5  13 - 8PSK 2/3  14 - 8PSK 3/4  15 - 8PSK 5/6  16 - 8PSK 8/9  17 - 8PSK 9/10</p> <p>18 - 16-APSK 2/3  19 - 16-APSK 3/4  20 - 16-APSK 4/5  21 - 16-APSK 5/6  22 - 16-APSK 8/9  23 - 16-APSK 9/10</p> <p>24 - 32-APSK 3/4  25 - 32-APSK 4/5  26 - 32-APSK 5/6  27 - 32-APSK 8/9  28 - 32-APSK 9/10</p>
ipilot	1	<p>pilot mode:</p> <p>0 - without pilot  1 - with pilot</p>
irdy	1	Modulator output data request.
irroll	2	<p>RRC filter roll-off factor:</p> <p>0 - alpha=0.35  1 - alpha=0.25  2 - alpha=0.2</p>
irst	1	The IP Core synchronously reset when irst is asserted high.
isample	32	<p>bandwidth control (symbol rate):</p> <p>0.01% to 25% of iclk</p>
isize	1	<p>LDPC frame size:</p> <p>0 - Normal FECFrame (Nldpc = 64800 bits)  1 - Short FECFrame (Nldpc = 16200 bits)</p>

isop	1	input sync-word byte marker (0x47 TS)
ival	1	input data valid
odati	W_DAC	modulator output at baseband (I channel) or at an intermediate frequency
odatq	W_DAC	modulator output at baseband (Q channel)
ordy	1	ready to accept input data

IP Core  
Parameters

Table 2 describes the DVB-S2 Modulator IP Core parameters, which must be set before synthesis.

Table 2. The DVB-S2 Modulator IP Core parameters description	
Parameter	Description
W_DAC	Width of output DAC symbols ( <b>odati/odatq</b> ) Increasing the width of odati/odatq, increases the quality of waveform but also increases FPGA required resource

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the DVB-S2 Modulator IP Core measurement results.

Table 3. The DVB-S2 Modulator performance				
IP Core parameters	FPGA type			
	Resource	Speed grade, maximal system frequency		
W_DAC=16	Altera Cyclone V 5CEFA7			
	4648 ALMs (9%) 50 M10K RAM blocks (8%) 14 DSP (18x18) (9%)	-8, Fmax	-7, Fmax	-6, Fmax
		118.0 MHz 29.5 Msymb/s	138.0 MHz 34.5 Msymb/s	156.0 MHz 39.0 Msymb/s
W_DAC=16	Xilinx Virtex-7 XC7VX330T			
	2502 Slices (5%) 26 18K RAM blocks (2%) 14 DSP (18x18) (2%)	-1, Fmax	-2, Fmax	-3, Fmax
		206.0 MHz 51.5 Msymb/s	258.0 MHz 64.5 Msymb/s	269.0 MHz 67.25 Msymb/s

IP Core Interface Description

IP core has two ways of forming the output spectrum:

- Baseband (using **odati** and **odatq**), **ifreq** equal 0
- Intermediate frequency (using **odati**), **ifreq** not equal 0

Digital-to-analog converters must operate synchronously with the DVB-S2 Modulator IP core. Figure 3 shows the DAC connection diagram for baseband mode and Figure 4 shows the timing diagram for this mode.

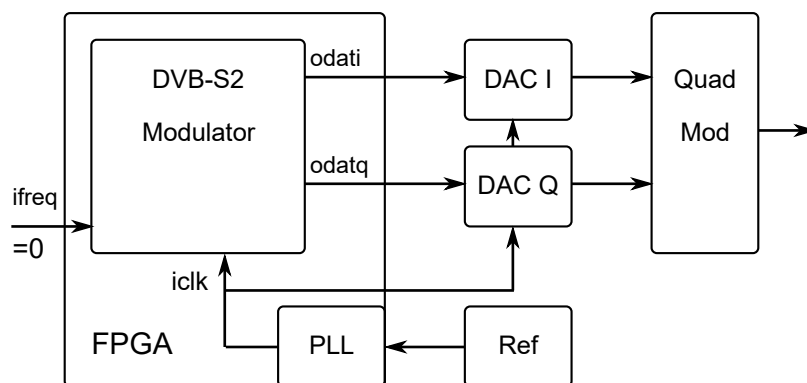
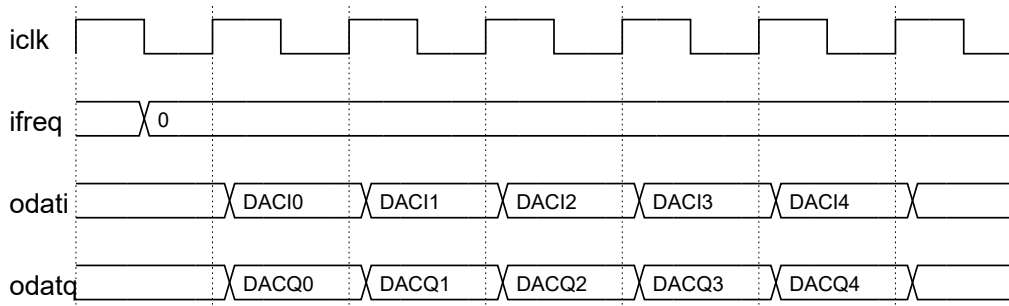
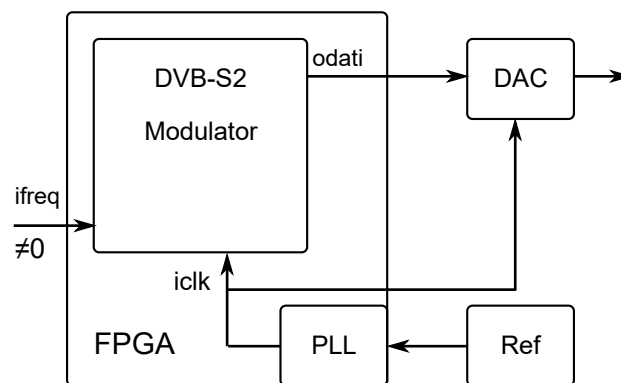


Figure 3. The DAC connection diagram for baseband mode.

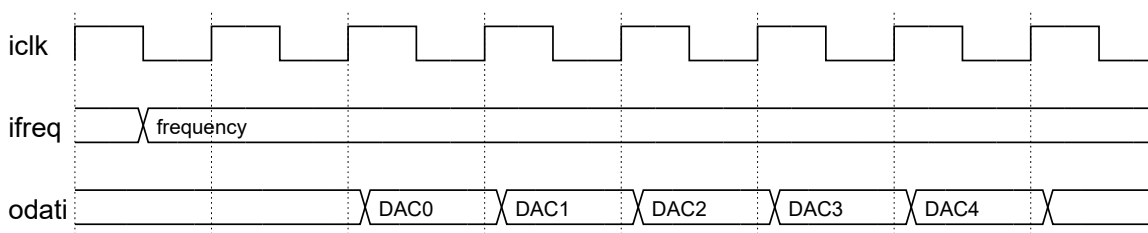


**Figure 4. The timing diagram for baseband mode.**

Figure 5 shows the DAC connection diagram for IF mode and Figure 6 shows the timing diagram for this mode. The output intermediate frequency port **ifreq** sets the central frequency for **odati** modulator output port.

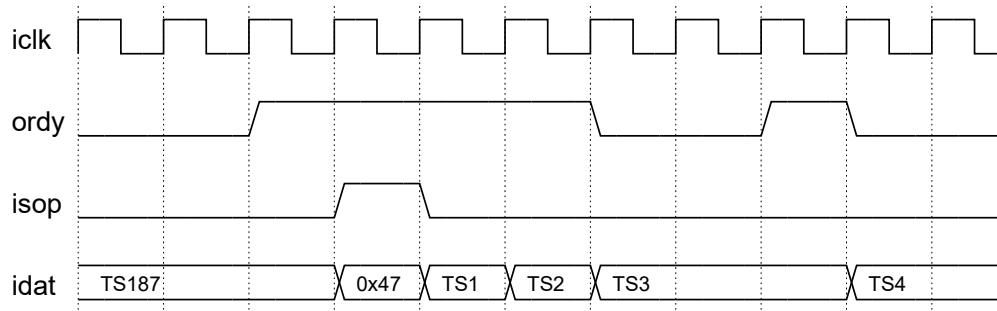


**Figure 5. The DAC connection diagram for IF mode.**



**Figure 6. The timing diagram for IF mode.**

Figure 7 shows an example of the waveform of the input interface. Handshake port **ordy** controls input dataflow. Input data is read from the input **idat** only when **ordy** is equal to logical one ("1").



**Figure 7. The timing diagram of the IP Core input interface.**



## Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

<https://www.iprium.com/ipcores/id/dvbs2-modulator/>

## Feedback

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## Revision history

Version	Date	Changes
5.0	2017.11.14	Added support for AD9361, AD9363, AD9364, AD9371, AD9375 and AD9789
4.0	2016.02.23	Added DUMMY frame support for VCM/ACM mode
3.1	2015.02.02	Added support for 16-APSK and 32-APSK modulation with CCM/VCM/ACM mode
3.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
2.0	2014.03.19	MER and C/I improvements
1.0	2011.06.06	Official release