DVB-S Modulator IP Core Specification

Release Information

Name	DVB-S Modulator IP Core
Version	3.0
Build date	2017.11
Ordering code	ip-dvbs-modulator
Specification revision	r1620

Features

The IP core is full-featured digital DVB-S modulator and is fully compatible with this standard:

- ETSI EN 300 421 (v1.1.2)

Price and License

Price:

- Netlist price : 2180 EUR
- Source code price : 15900 EUR
- +10% of the cost for each additional FPGA family netlist
- Customization price is 1000-5000 EUR

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The DVB-S Modulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the DVB-S Modulator IP Core block diagram.

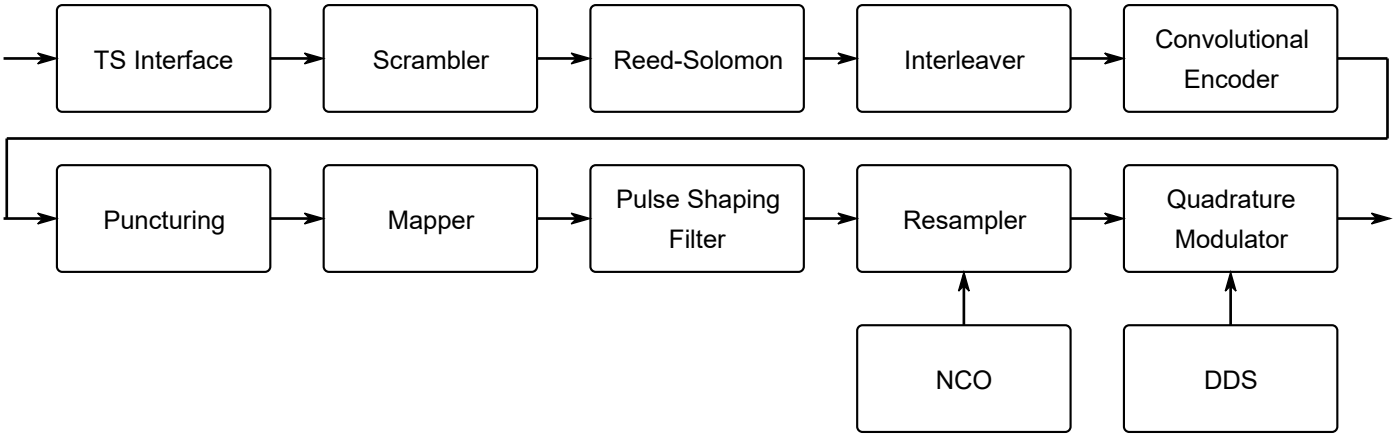

Figure 1. The DVB-S Modulator IP Core block diagram

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the DVB-S Modulator IP Core.

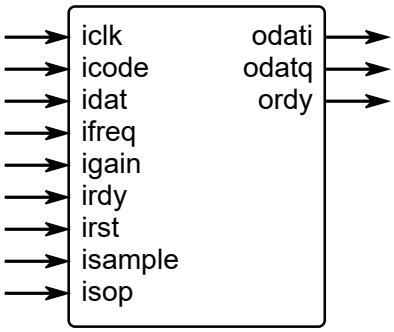

Figure 2. The DVB-S Modulator port map

Table 1. The DVB-S Modulator port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
icode	3	code rate: 0 - 1/2 1 - 2/3 2 - 3/4 3 - 5/6 4 - 7/8
idat	8	input (information) data
ifreq	32	output intermediate frequency
igain	W_DAC	output gain control
irdy	1	Modulator output data request.

irst	1	The IP Core synchronously reset when irst is asserted high.
isample	32	bandwidth control (symbol rate): 0.01% to 25% of iclk
isop	1	input sync-word byte marker (0x47 TS)
odati	W_DAC	modulator output at baseband (I channel) or at an intermediate frequency
odatq	W_DAC	modulator output at baseband (Q channel)
ordy	1	ready to accept input data

IP Core Parameters

Table 2 describes the DVB-S Modulator IP Core parameters, which must be set before synthesis.

Table 2. The DVB-S Modulator IP Core parameters description

Parameter	Description
W_DAC	Width of output DAC symbols (**odati/odatq**) Increasing the width of odati/odatq, increases the quality of waveform but also increases FPGA required resource

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the DVB-S Modulator IP Core measurement results.

Table 3. The DVB-S Modulator performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_DAC=16	Altera Cyclone V 5CEFA7			
	2044 ALMs (4%) 5 M10K RAM blocks (1%) 12 DSP (18x18) (8%)	-8, Fmax	-7, Fmax	-6, Fmax
		144.0 MHz 36.0 Msymb/s	170.0 MHz 42.5 Msymb/s	204.0 MHz 51.0 Msymb/s
W_DAC=16	Xilinx Virtex-7 XC7VX330T			
	1163 Slices (3%) 3 18K RAM blocks (1%) 12 DSP (18x18) (2%)	-1, Fmax	-2, Fmax	-3, Fmax
		230.0 MHz 57.5 Msymb/s	297.0 MHz 74.25 Msymb/s	310.0 MHz 77.5 Msymb/s

IP Core Interface Description

IP core has two ways of forming the output spectrum:

- Baseband (using **odati** and **odatq**), **ifreq** equal 0
- Intermediate frequency (using **odati**), **ifreq** not equal 0

Digital-to-analog converters must operate synchronously with the DVB-S Modulator IP core. Figure 3 shows the DAC connection diagram for baseband mode and Figure 4 shows the timing diagram for this mode.

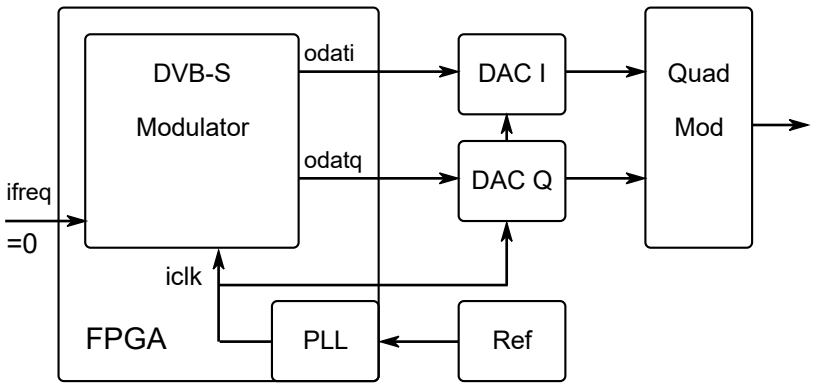

Figure 3. The DAC connection diagram for baseband mode.

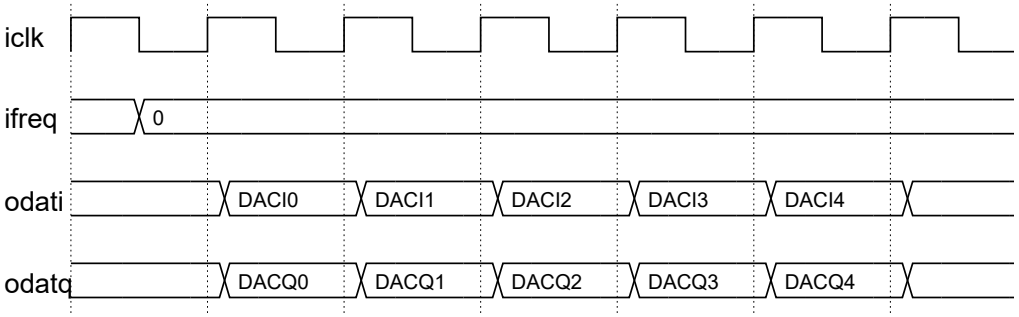

Figure 4. The timing diagram for baseband mode.

Figure 5 shows the DAC connection diagram for IF mode and Figure 6 shows the timing diagram for this mode. The output intermediate frequency port **ifreq** sets the central frequency for **odati** modulator output port.

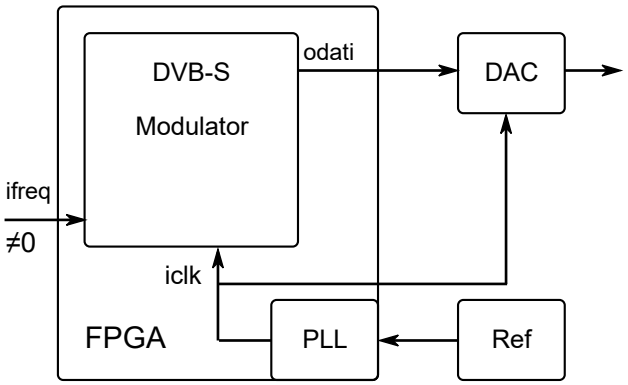

Figure 5. The DAC connection diagram for IF mode.

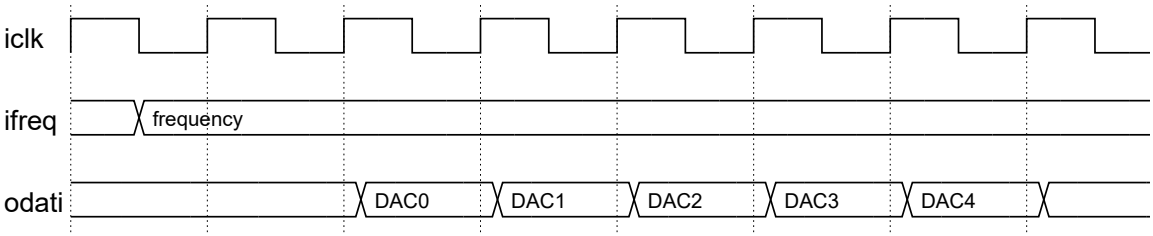

Figure 6. The timing diagram for IF mode.

Figure 7 shows an example of the waveform of the input interface. Handshake port **ordy** controls input dataflow. Input data is read from the input **idat** only when **ordy** is equal to logical one ("1").

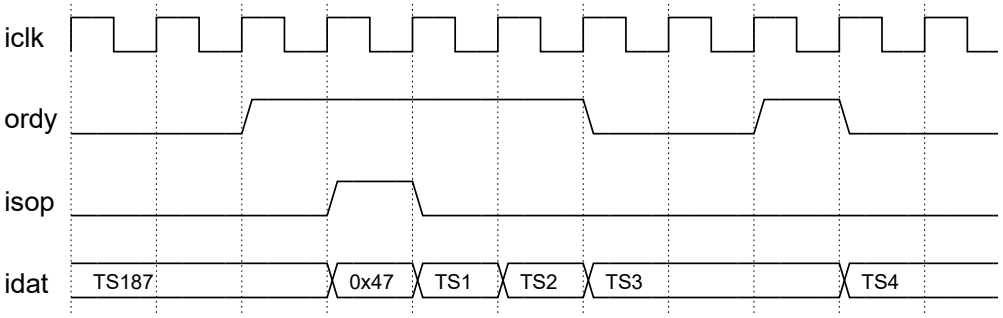

Figure 7. The timing diagram of the IP Core input interface.

Response time to changes in the output mode of the DVB-S modulator through **icode**, **isample** ports is not more than one thousand (1,000) DVB-S symbols. Proper forming of the DVB-S spectrum within one thousand (1,000) symbols after the configuration change is not guaranteed.

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/dvbs-modulator/

Feedback

IPrium LLC

39, via Umberto I, Ischitella (FG), 71010, Italy

Tel.: +39-375-6429155

E-mail: info@iprium.com

Skype: fpgahelp

website: https://www.iprium.com/contacts/

Revision history

Version	Date	Changes
3.0	2017.11.14	Added support for AD9361, AD9363, AD9364, AD9371, AD9375 and AD9789
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.1	2010.12.23	Maintenance improvements
1.0	2010.12.03	Official release