



DVB-T Modulator IP Core
Specification

Release Information

Name	DVB-T Modulator IP Core
Version	2.1
Build date	2015.07
Ordering code	ip-dvbt-modulator
Specification revision	r1465

Features

The IP core is full-featured digital DVB-T modulator and is fully compatible with this standard:

- ETSI EN 300 744 (v1.6.1)

Deliverables

The DVB-T Modulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the DVB-T Modulator IP Core block diagram.

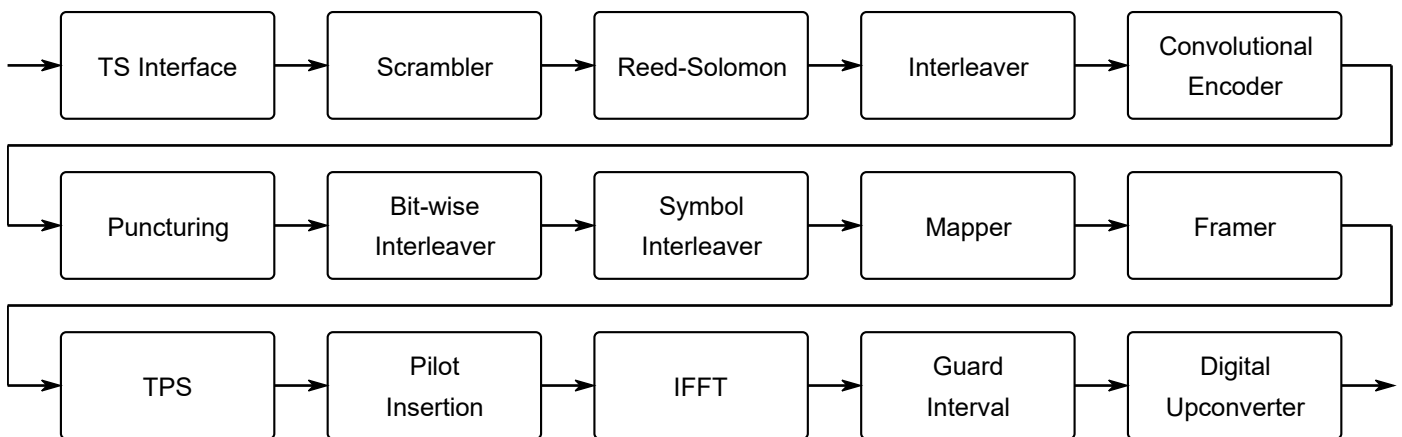


Figure 1. The DVB-T Modulator IP Core block diagram

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the DVB-T Modulator IP Core.

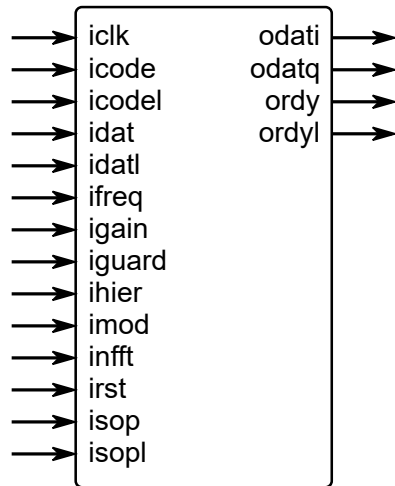


Figure 2. The DVB-T Modulator port map

Table 1. The DVB-T Modulator port map description		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
icode icodel	3	code rate for HP and LP streams: 0 - 1/2 1 - 2/3 2 - 3/4 3 - 5/6 4 - 7/8
idat	8	input (information) data for HP stream
idatl	8	input (information) data for LP stream if hiearchy modulation enabled
ifreq	32	output intermediate frequency
igain	16	output gain control
iguard	2	guard interval: 0 - 1/32 1 - 1/16 2 - 1/8 3 - 1/4
ihier	2	Hierarchy mode enable and Alpha choose: 0 - Non-hierarchy 1 - Hierarchy, Alpha = 1 2 - Hierarchy, Alpha = 2 3 - Hierarchy, Alpha = 4

imod	2	Modulation: 0 - QPSK 1 - 16-QAM 2 - 64-QAM
infft	1	Choose number of subcarriers: 0 - 2K Mode 1 - 8K Mode
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	input sync-word byte marker (0x47 TS) for HP stream
isopl	1	input sync-word byte marker (0x47 TS) for LP stream
odati	W_DAC	modulator output at baseband (I channel) or at an intermediate frequency
odatq	W_DAC	modulator output at baseband (Q channel)
ordy	1	ready to accept input data for HP stream
ordyl	1	ready to accept input data for LP stream

IP Core Parameters

Table 2 describes the DVB-T Modulator IP Core parameters, which must be set before synthesis.

Table 2. The DVB-T Modulator IP Core parameters description	
Parameter	Description
MODE	Supported mode of operation: Non-hierarchy 8 MHz (default), Hierarchy (+30% to the IP Core price), 6/7/8 MHz (+30% to the IP Core price), Full (+50% to the IP Core price).
W_DAC	Width of output DAC symbols (odati/odatq) Increasing the width of odati/odatq , increases the quality of waveform but also increases FPGA required resource

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the DVB-T Modulator IP Core measurement results.

Table 3. The DVB-T Modulator performance				
IP Core parameters	FPGA type			
	Resource	Speed grade, maximal system frequency		
MODE = 2K-only W_DAC=16	Altera Cyclone V 5CEFA7			
	2478 ALMs (5%) 66 M10K RAM blocks (10%) 12 DSP (18x18) (8%)	-8, Fmax	-7, Fmax	-6, Fmax
		enough for spectrum bandwidth 1.7/5/6/7/8 MHz		
MODE = 2K-only W_DAC=16	Xilinx Virtex-7 XC7VX330T			
	1806 Slices (4%) 28 18K RAM blocks (2%) 12 DSP (18x18) (2%)	-1, Fmax	-2, Fmax	-3, Fmax
		enough for spectrum bandwidth 1.7/5/6/7/8/10 MHz		

IP Core Interface Description

IP core has two ways of forming the output spectrum:

- Baseband (using **odati** and **odatq**), **ifreq** equal 0
- Intermediate frequency (using **odati**), **ifreq** not equal 0

Digital-to-analog converters must operate synchronously with the DVB-T Modulator IP core. Figure 3 shows the DAC connection diagram for baseband mode and Figure 4 shows the timing diagram for this mode.

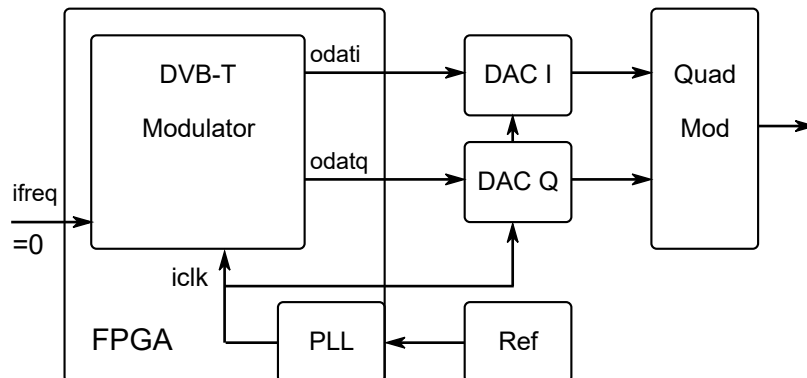


Figure 3. The DAC connection diagram for baseband mode.

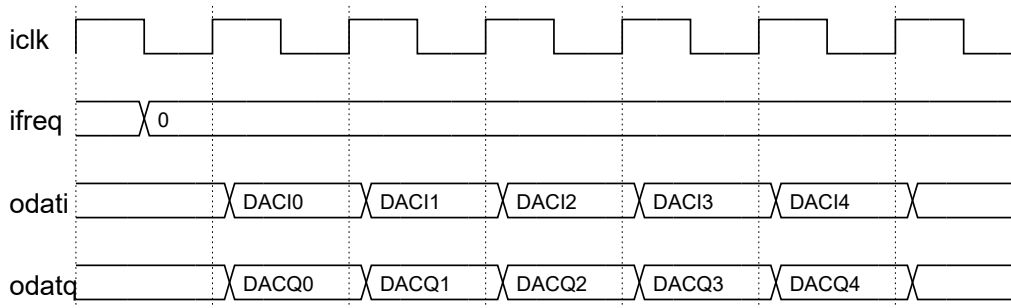


Figure 4. The timing diagram for baseband mode.

Figure 5 shows the DAC connection diagram for IF mode and Figure 6 shows the timing diagram for this mode. The output intermediate frequency port **ifreq** sets the central frequency for **odati** modulator output port.

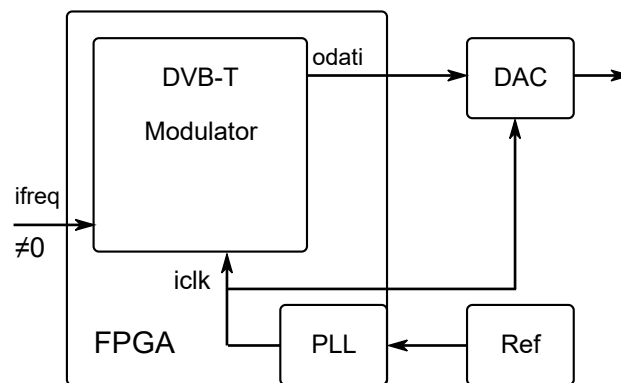


Figure 5. The DAC connection diagram for IF mode.

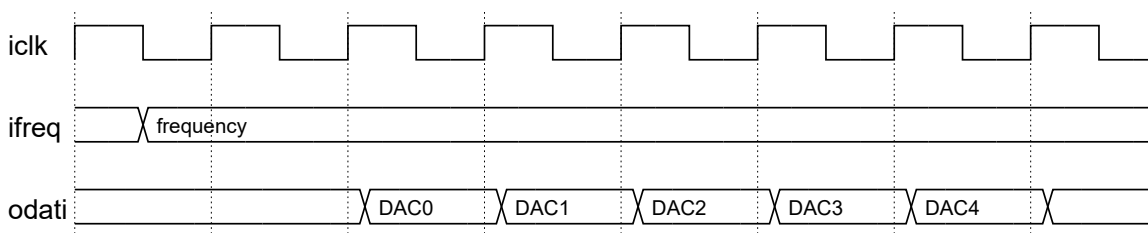


Figure 6. The timing diagram for IF mode.

Figure 7 shows an example of the waveform of the input interface. Handshake port **ordy** controls input dataflow. Input data is read from the input **idat** only when **ordy** is equal to logical one ("1").

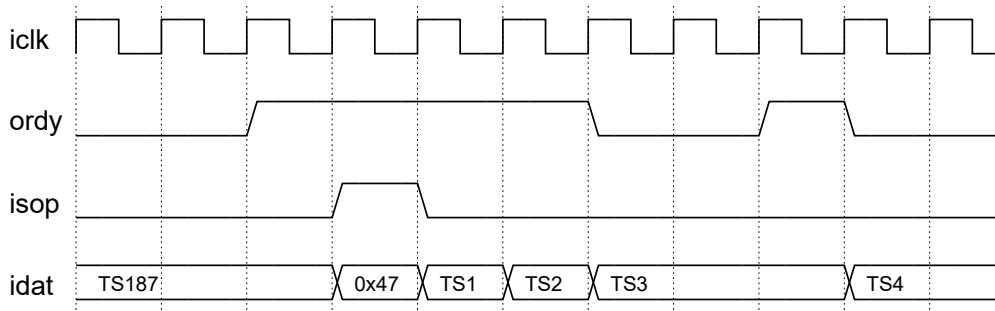


Figure 7. The timing diagram of the IP Core input interface.

Response time to changes in the output mode of the DVB-T modulator through **icode**, **iguard**, **imod** ports is not more than ten (10) DVB-T super-frames. Proper forming of the DVB-T spectrum within ten (10) super-frames after the configuration change is not guaranteed.

For the formation of the spectrum width input clock frequency must be exactly equal:

- For 10 MHz - **iclk** = $80/7 * 16 = 182.85714$ MHz
- For 8 MHz - **iclk** = $64/7 * 16 = 146.28571$ MHz
- For 7 MHz - **iclk** = $64/8 * 16 = 128.00000$ MHz
- For 6 MHz - **iclk** = $48/7 * 16 = 109.71429$ MHz
- For 5 MHz - **iclk** = $40/7 * 16 = 91.42857$ MHz
- For 1.7 MHz - **iclk** = $131/71 * 16 = 29.52113$ MHz

Quality Metrics

The DVB-T Modulator IP Core provides the following quality metrics:

- Full compliance with the ETSI EN 300 744 Standard
- 50 dB MER
- -90 dBc out-of-band emission

Quality metrics of the IP Core can be improved on request.

Figure 8 shows the DVB-T Modulator IP Core signal spectrum before digital upconverter (DUC).

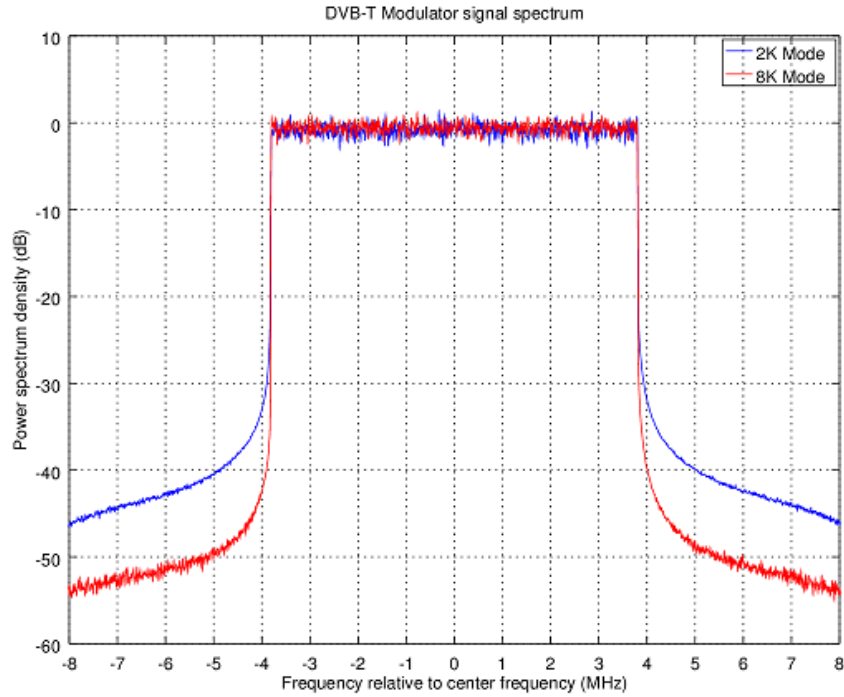


Figure 8. DVB-T transmission signal spectrum before DUC.

Figure 9 shows the DVB-T Modulator IP Core signal spectrum after DUC.

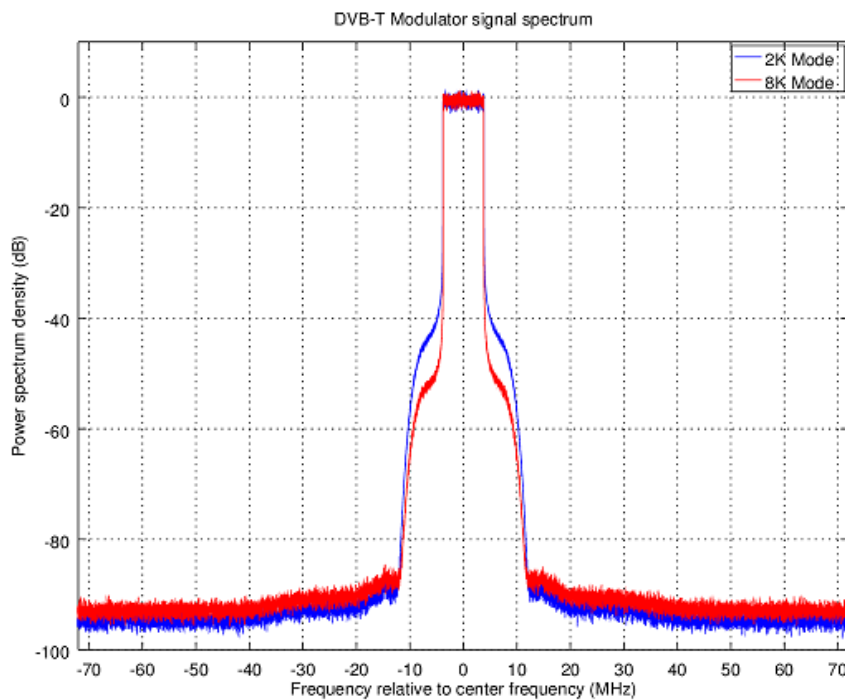


Figure 9. DVB-T signal spectrum after DUC.

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

<https://www.iprium.com/ipcores/id/dvbt-modulator/>

Feedback

IPrium LLC

39, via Umberto I, Ischitella (FG), 71010, Italy

Tel.: +39-375-6429155

E-mail: info@iprium.com

Skype: fpgahelp

website: <https://www.iprium.com/contacts/>

Revision history

Version	Date	Changes
2.1	2015.07.14	Improved MER and SFDR
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.1	2010.12.27	Maintenance improvements
1.0	2010.12.03	Official release