IPRIUM

G.709 Encoder/Decoder IP Core Specification

Release Information

Name	G.709 Codec IP Core
Version	2.1
Build date	2015.03
Ordering code	ip-g709-codec
Specification revision	r1620

Features

The IP core implements the Reed-Solomon (255, 239) forward error correction algorithm for optical lines and is fully compatible with this recommendation:

- ITU-T G.709 (2.5G, 10G and 40G optical networks)

Price and License

Price:

- Netlist price : 1080 EUR
- Source code price : 10400 EUR
- +10% of the cost for each additional FPGA family netlist
- Customization price is 1000-5000 EUR

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The G.709 Encoder/Decoder IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the G.709 Encoder IP Core block diagram.

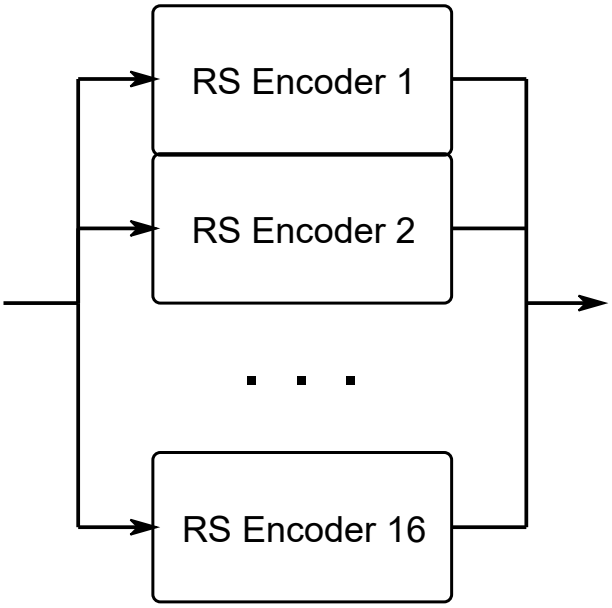

Figure 1. The G.709 Encoder IP Core block diagram

The G.709 Encoder consists of 16 parallel Reed-Solomon encoders (255, 239) m = 8 with generator polynomial = 285.

Figure 2 shows the G.709 Decoder IP Core block diagram.

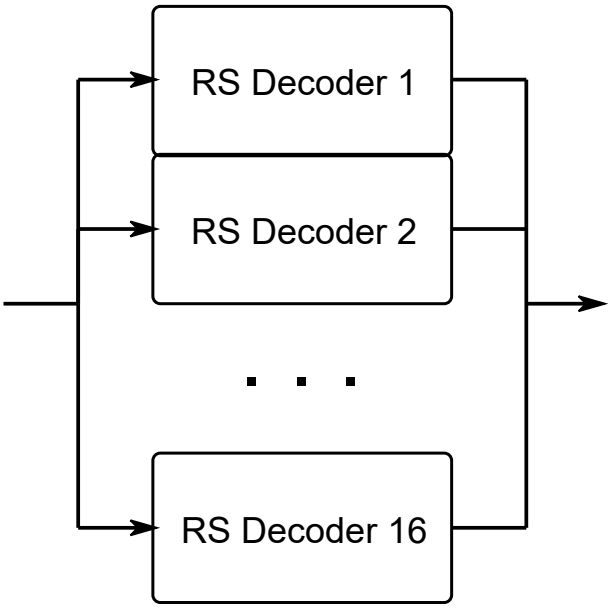

Figure 2. The G.709 Decoder IP Core block diagram

The G.709 Decoder consists of 16 parallel Reed-Solomon decoders (255, 239) m = 8 with generator polynomial = 285.

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the G.709 Encoder IP Core.

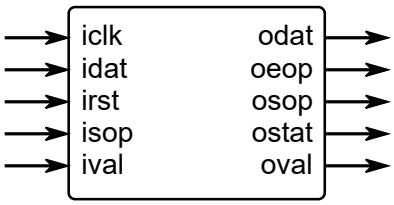

Figure 3. The G.709 Encoder port map

Table 1. The G.709 Encoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	128	Input (information) data.
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	Start of information packet marker.
ival	1	Input data valid.
odat	128	Output (encoded) data.
oeop	1	End of encoded packet marker.
osop	1	Start of encoded packet marker.
ostat	2	Status of encoded packet: 0 - no data output 1 - information data output 2 - parity data output
oval	1	Output data valid.

Figure 4 shows a graphic symbol, and Table 2 describes the ports of the G.709 Decoder IP Core.

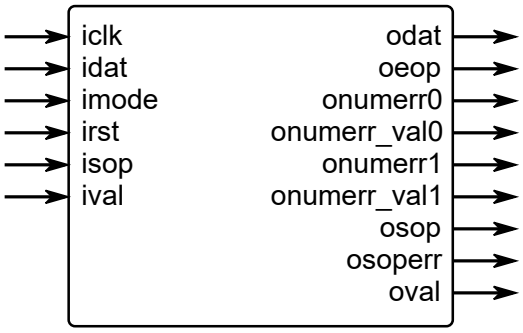

Figure 4. The G.709 Decoder port map

Table 2. The G.709 Decoder port map description		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	128	Input (encoded) data.
imode	1	Decoded data output mode: 0 - without correction (bypass) 1 - with error correction
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	Start of coded packet marker.
ival	1	Input data valid.
odat	128	Output (decoded) data.
oeop	1	End of decoded packet marker.
onumerr0	5	Number of input blocks with errors.
onumerr_val0	1	Onumerr0 valid.
onumerr1	5	Number of output blocks with errors.
onumerr_val1	1	Onumerr1 valid.
osop	1	Start of decoded packet marker.
osoperr	1	Set "1" when isop period error.
oval	1	Output data valid.

IP Core Operation Description

The G.709 Encoder/Decoder IP Core is in full accordance with ITU-T G.709/Y.1331 (12/2009) "Annex A. Forward error correction using 16-byte interleaved RS(255,239) codecs". The IP Core is designed for operation with the OTN OTU2 linear stream at 10.7 Gbps in fiber optic communication systems. The G.709 Encoder/Decoder IP Core can be used in both continuous and burst modes.

Key features of the IP Core:

- Exact accordance with the recommendation ITU-T G.709
- Synchronous, high-speed decoding algorithm
- Output ports of error statistics (input and output errors)
- Encoding delay is 1 cycle
- Decoding delay is 769 cycles (9.2 us)

IP Core Parameters

Table 3 describes the G.709 Encoder/Decoder IP Core parameters, which must be set before synthesis.

Table 3. The G.709 Encoder/Decoder IP Core parameters description	
Parameter	Description
There are no parameters available to change	

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the G.709 Encoder IP Core measurement results.

Table 4. The G.709 Encoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
	Altera Cyclone V 5CEFA7			
	1351 ALMs (3%) 0 M10K RAM blocks (0%) 0 DSP (18x18) (0%)	-8, Fmax	-7, Fmax	-6, Fmax
		202.0 MHz 25.0 Gbps	231.0 MHz 29.0 Gbps	259.0 MHz 32.0 Gbps
	Xilinx Virtex-7 XC7VX330T			
	925 Slices (2%) 0 18K RAM blocks (0%) 0 DSP (18x18) (0%)	-1, Fmax	-2, Fmax	-3, Fmax
		357.0 MHz 45.0 Gbps	430.0 MHz 55.0 Gbps	513.0 MHz 65.0 Gbps

Table 5 summarizes the G.709 Decoder IP Core measurement results.

Table 5. The G.709 Decoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
	Altera Cyclone V 5CEFA7			
	13833 ALMs (25%) 48 M10K RAM blocks (7%) 0 DSP (18x18) (0%)	-8, Fmax	-7, Fmax	-6, Fmax
		165.0 MHz 21.0 Gbps	187.0 MHz 23.0 Gbps	208.0 MHz 26.0 Gbps
	Xilinx Virtex-7 XC7VX330T			
	8253 Slices (17%) 48 18K RAM blocks (14%) 0 DSP (18x18) (0%)	-1, Fmax	-2, Fmax	-3, Fmax
		223.0 MHz 28.0 Gbps	273.0 MHz 34.0 Gbps	319.0 MHz 40.0 Gbps

IP Core Interface Description

The encoder recognizes the first information symbol by the **isop** "start of information block" marker of that symbol (FAS OH = 0xF6F6F6282828). The bit width of input data **idat** and output data **odat** is 128 bits. The codec throughput of 10.7 Gbps requires a timing frequency of at least 85 MHz. The resulting encoded block at the encoder output can be recognized by the **osop** "start of encoded block" marker. Additionally the encoder marks the status of the output data by **ostat**:

- 0 - no data output
- 1 - information symbols of encoded block
- 2 - parity (check) symbols of encoded block

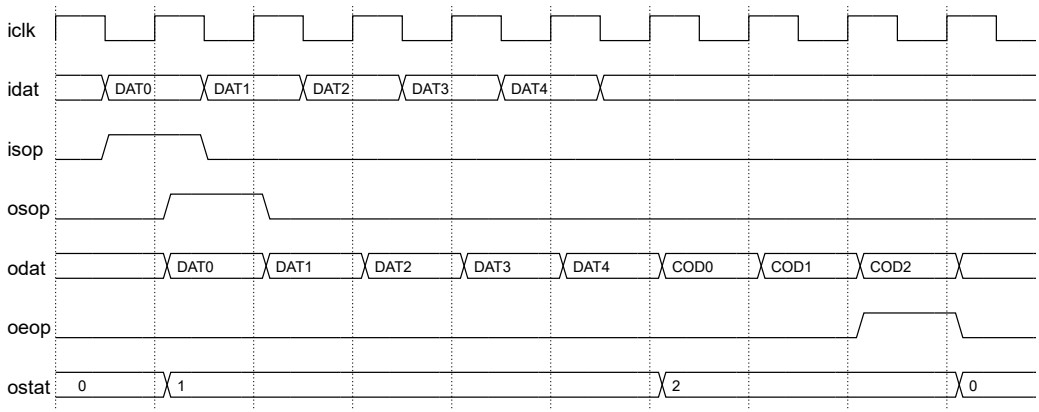

Figure 5. The timing diagrams of the G.709 Encoder operation

Quality Metrics

The error-correcting capability of the G.709 Codec IP Core is shown on the figure 6.

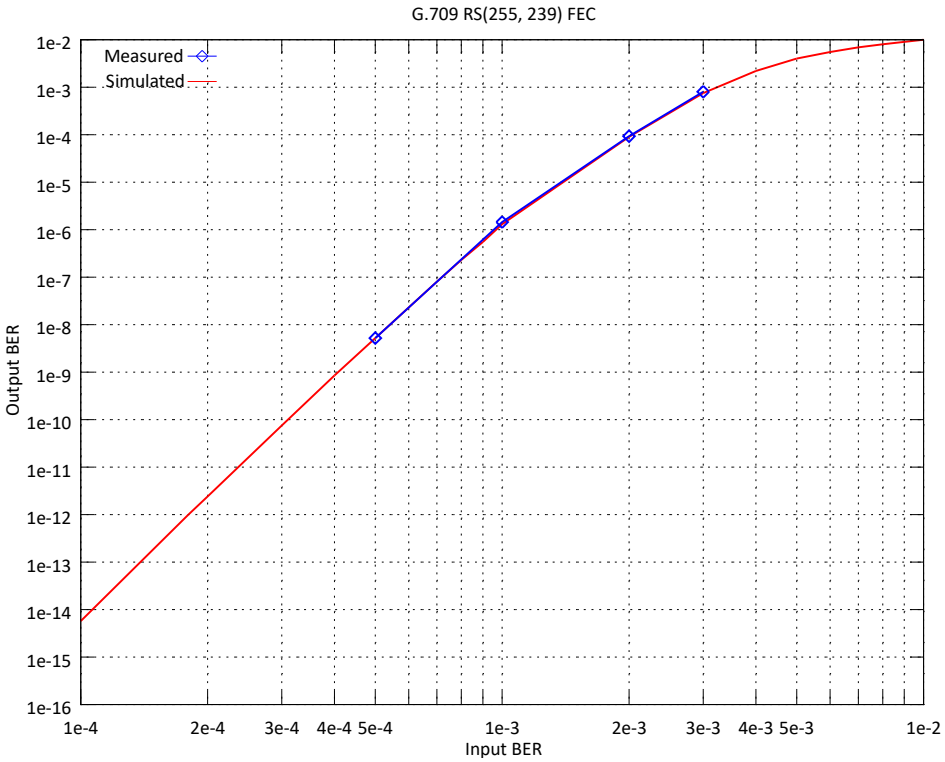

Figure 6. The error-correcting capability of the G.709 Codec

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/g709-codec/

Feedback

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Revision history

Version	Date	Changes
2.1	2015.03.27	Updated resources and performance information of the IP Core.
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.0	2012.10.23	Official release