I.6 LDPC Encoder/Decoder IP Core Specification

Release Information

Name	I.6 LDPC Codec IP Core
Version	2.0
Build date	2014.09
Ordering code	ip-i6-ldpc-codec
Specification revision	r1620

Features

The IP core implements the LDPC (32640, 30592) forward error correction algorithm for optical lines and is fully compatible with this recommendation:

- ITU-T G.975.1 (super-FEC for 2.5G, 10G and 40G optical networks)

Price and License

Price:

- Netlist price : 5460 EUR
- Source code price : 32300 EUR
- +10% of the cost for each additional FPGA family netlist
- Customization price is 1000-5000 EUR

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The I.6 LDPC Encoder/Decoder IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the I.6 LDPC Encoder IP Core block diagram.

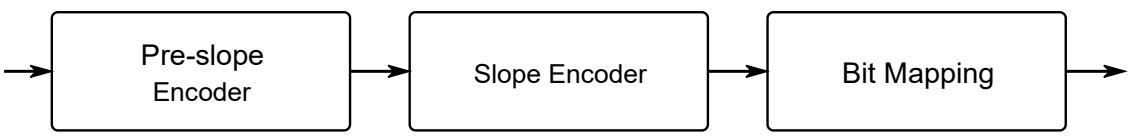

Figure 1. The I.6 LDPC Encoder IP Core block diagram

The I.6 LDPC Encoder consists of a Pre-slope Encoder module (**Pre-**

slope Encoder), a Slope Encoder module (**Slope Encoder**) and a Bit Mapping module (**Bit Mapping**).

Figure 2 shows a block diagram of one I.6 LDPC Decoder IP Core decoding iteration.

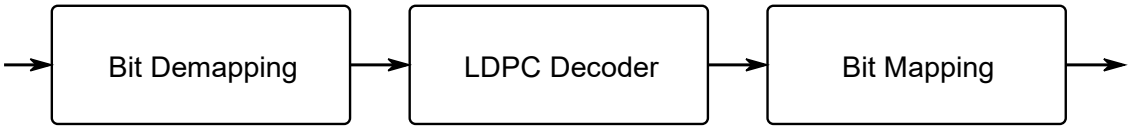

Figure 2. Block diagram of one I.6 LDPC Decoder iteration

The I.6 LDPC Decoder architecture makes it possible to specify a random number of decoding iterations. A decoding iteration consists of a Bit Demapping module (**Bit Demapping**), a LDPC Decoder module (**LDPC Decoder**) and a Bit Mapping module (**Bit Mapping**).

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the I.6 LDPC Encoder IP Core.

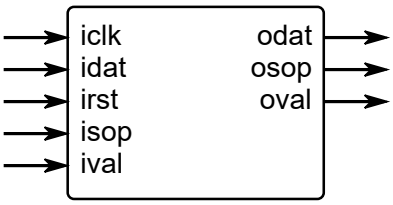

Figure 3. The I.6 LDPC Encoder port map

Table 1. The I.6 LDPC Encoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	64	input (information) data
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of information packet marker
ival	1	input data valid
odat	64	output (encoded) data
osop	1	start of encoded packet marker

oval	1	output data valid

Figure 4 shows a graphic symbol, and Table 2 gives a description of the I.6 LDPC Decoder IP Core ports.

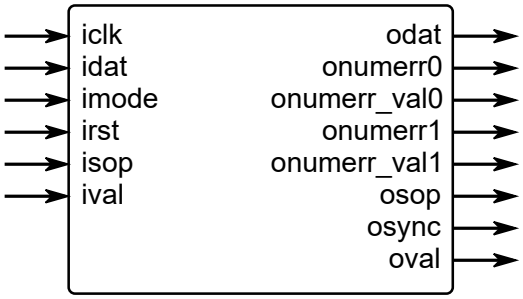

Figure 4. The I.6 LDPC Decoder port map

Table 2. The I.6 LDPC Decoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	64	input (encoded) data
imode	1	decoded data output mode: 0 - without correction (bypass) 1 - with error correction
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of coded packet marker
ival	1	input data valid
odat	64	output (decoded) data
onumerr0	5	number of input blocks with errors
onumerr_val0	1	onumerr0 valid
onumerr1	5	number of output blocks with errors
onumerr_val1	1	onumerr1 valid
osop	1	start of decoded packet marker
osync	1	correct isop with FAS input
oval	1	output data valid

IP Core Operation Description

The I.6 LDPC Encoder/Decoder IP Core is in full accordance with the recommendation ITU-T G.975.1 (02/2004) "Appendix I. Super FEC schemes. I.6 LDPC super FEC code". The IP Core is designed for operation with the OTN OTU2 linear stream at 10.7 Gbps in fiber optic communication systems. The I.6 LDPC Encoder/Decoder IP Core can be used in both continuous and burst modes.

Key features of the IP Core:

- Exact accordance with the recommendation ITU-T G.975.1 I.6
- Synchronous, high-speed decoding algorithm
- Output ports of error statistics (input and output errors)
- Encoding delay is 1,020 cycles (6.08 us)
- Decoding delay of 12 iterations (12 slope decoding) is 2,009 cycles (12.028 us)

IP Core Parameters

Table 3 describes the I.6 LDPC Encoder/Decoder IP Core parameters, which must be set before synthesis.

Table 3. The I.6 LDPC Encoder/Decoder IP Core parameters description

Parameter	Description
ITER	number of decoding iterations
s1, ..., s7	slope coefficients

Example:

- ITER = 5 means five iterative decoding iterations:

idat - dec1 - dec2 - dec3 - dec4 - dec5 - odat

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the I.6 LDPC Encoder IP Core measurement results.

Table 4. The I.6 LDPC Encoder performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
10G mode	Altera Cyclone IV EP4CE115			
	- LEs - M9K	-9L, Fmax	-8, Fmax	-7, Fmax
		—	—	—
10G mode	Xilinx Virtex-6 XC6VLX240T			
	- Slices - 18K RAM blocks	-1, Fmax	-2, Fmax	-3, Fmax
		—	—	—

Table 5 summarizes the I.6 LDPC Decoder IP Core measurement results.

Table 5. The I.6 LDPC Decoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
10G mode 12 iterations	Altera Cyclone IV EP4CE115			
	39,995 LEs 36 M9K	-9L, Fmax	-8, Fmax	-7, Fmax
		82.65 MHz 5.3 Gbps	109.9 MHz 7.0 Gbps	125.71 MHz 8.0 Gbps
10G mode 12 iterations	Xilinx Virtex-6 XC6VLX240T			
	7,192 Slices 36 18K RAM blocks	-1, Fmax	-2, Fmax	-3, Fmax
		159.2 MHz 10.2 Gbps	186.0 MHz 11.9 Gbps	190.2 MHz 12.2 Gbps

IP Core Interface Description

The encoder recognizes the first information symbol by the **isop** "start of information block" marker of that symbol (FAS OH = 0xF6F6F6282828). The bit width of input data **idat** and output data **odat** is 64 bits. The codec throughput of 10.7 Gbps requires a timing frequency of at least 170 MHz. The resulting encoded block at the encoder output can be recognized by the **osop** "start of encoded block" marker.

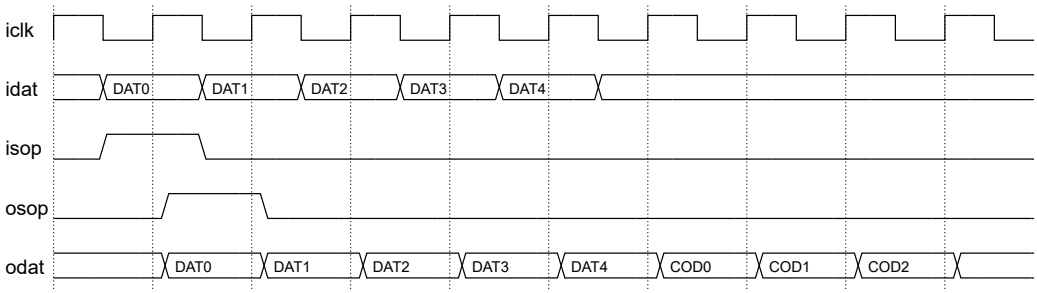

Figure 5. The timing diagrams of the I.6 LDPC Encoder operation

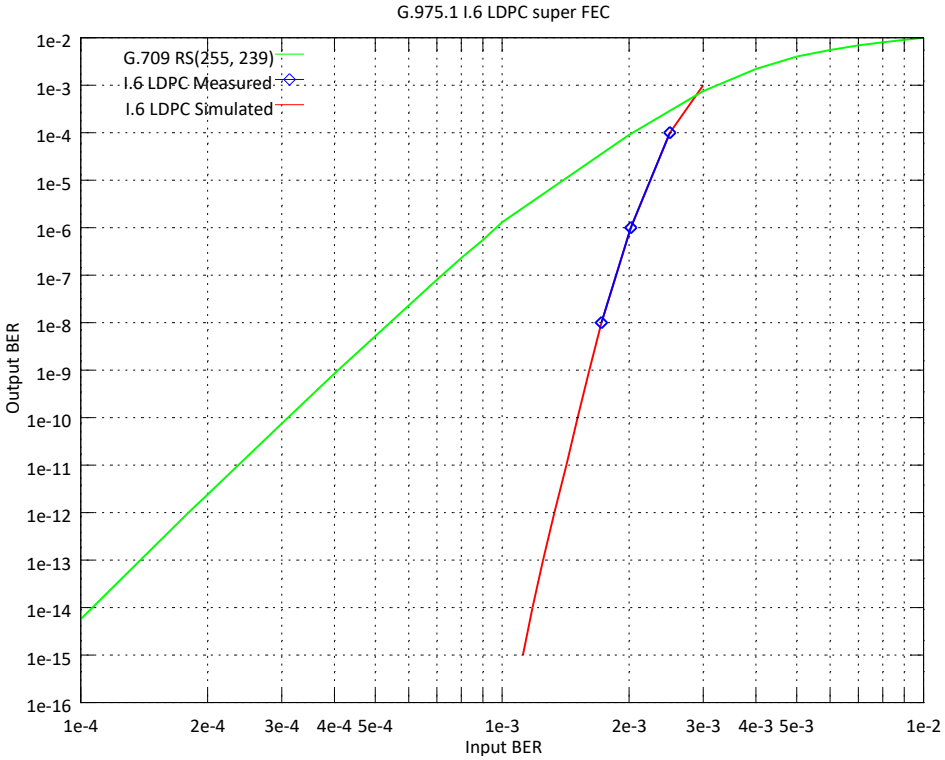

Figure 6. The error-correcting capability of the I.6 LDPC Decoder

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/i6-ldpc-codec/

Feedback

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Revision history

Version	Date	Changes
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.0	2013.04.23	Official release