



## I.9 BCH Encoder/Decoder IP Core Specification

### Release Information

|                        |                       |
|------------------------|-----------------------|
| Name                   | I.9 BCH Codec IP Core |
| Version                | 2.1                   |
| Build date             | 2015.05               |
| Ordering code          | ip-i9-bch-codec       |
| Specification revision | r1620                 |

### Features

The IP core implements the BCH (1020, 988) forward error correction algorithm for optical lines and is fully compatible with this recommendation:

- ITU-T G.975.1 (super-FEC for 2.5G, 10G and 40G optical networks)

### Price and License

Price:

- Netlist price : 7290 EUR
- Source code price : 41450 EUR
- +10% of the cost for each additional FPGA family netlist
- Customization price is 1000-5000 EUR

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

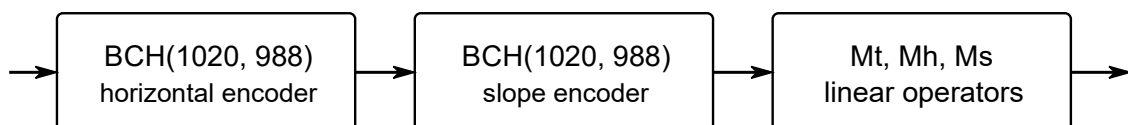
### Deliverables

The I.9 BCH Encoder/Decoder IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

### IP Core Structure

Figure 1 shows the I.9 BCH Encoder IP Core block diagram.

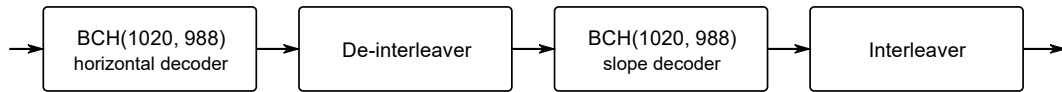


**Figure 1. The I.9 BCH Encoder IP Core block diagram**

The I.9 BCH Encoder consists of a horizontal BCH encoder

(BCH(1020, 988) horizontal encoder), a slope BCH encoder (BCH(1020, 988) slope encoder) and a linear conversion operators ( $M_t$ ,  $M_h$ ,  $M_s$  linear operators).

Figure 2 shows a block diagram of two I.9 BCH Decoder IP Core decoding iterations.

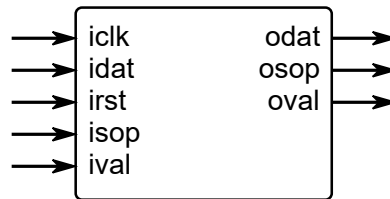


**Figure 2. Block diagram of two I.9 BCH Decoder IP Core decoding iterations**

The I.9 BCH Decoder architecture makes it possible to specify a random number of decoding iterations. Two decoding iterations consists of a horizontal BCH encoder (BCH(1020, 988) horizontal encoder), a deinterleaver module (De-interleaver), a slope BCH decoder (BCH(1020, 988) slope decoder) and an interleaver module (Interleaver).

### Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the I.9 BCH Encoder IP Core.

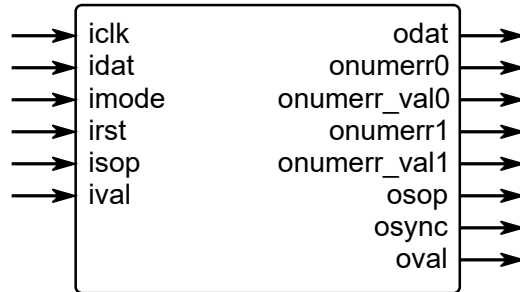


**Figure 3. The I.9 BCH Encoder port map**

| Table 1. The I.9 BCH Encoder port map description |       |                                                                         |
|---------------------------------------------------|-------|-------------------------------------------------------------------------|
| Port                                              | Width | Description                                                             |
| iclk                                              | 1     | The main system clock. The IP Core operates on the rising edge of iclk. |
| idat                                              | 64    | input (information) data                                                |
| irst                                              | 1     | The IP Core synchronously reset when irst is asserted high.             |
| isop                                              | 1     | start of information packet marker                                      |
| ival                                              | 1     | input data valid                                                        |
| odat                                              | 64    | output (encoded) data                                                   |

|      |   |                                |
|------|---|--------------------------------|
| osop | 1 | start of encoded packet marker |
| oval | 1 | output data valid              |

Figure 4 shows a graphic symbol, and Table 2 describes the ports of the I.9 BCH Decoder IP Core.



**Figure 4. The I.9 BCH Decoder port map**

| Table 2. The I.9 BCH Decoder port map description |       |                                                                                           |
|---------------------------------------------------|-------|-------------------------------------------------------------------------------------------|
| Port                                              | Width | Description                                                                               |
| iclk                                              | 1     | The main system clock. The IP Core operates on the rising edge of iclk.                   |
| idat                                              | 64    | input (encoded) data                                                                      |
| imode                                             | 1     | decoded data output mode:<br>0 - without correction (bypass)<br>1 - with error correction |
| irst                                              | 1     | The IP Core synchronously reset when irst is asserted high.                               |
| isop                                              | 1     | start of coded packet marker                                                              |
| ival                                              | 1     | input data valid                                                                          |
| odat                                              | 64    | output (decoded) data                                                                     |
| onumerr0                                          | 5     | number of input blocks with errors                                                        |
| onumerr_val0                                      | 1     | onumerr0 valid                                                                            |
| onumerr1                                          | 5     | number of output blocks with errors                                                       |
| onumerr_val1                                      | 1     | onumerr1 valid                                                                            |

|       |   |                                |
|-------|---|--------------------------------|
| osop  | 1 | start of decoded packet marker |
| osync | 1 | correct isop with FAS input    |
| oval  | 1 | output data valid              |

### IP Core Operation Description

The I.9 BCH Encoder/Decoder IP Core is in full accordance with the recommendation ITU-T G.975.1 (02/2004) "Appendix I. Super FEC schemes. I.9 Two interleaved extended BCH(1020,988) super FEC code". The IP Core is designed for operation with the OTN OTU2 linear stream at 10.7 Gbps in fiber optic communication systems. The I.39 BCH Encoder/Decoder IP Core can be used in both continuous and burst modes.

Key features of the IP Core:

- Exact accordance with the recommendation ITU-T G.975.1 I.9
- Synchronous, high-speed decoding algorithm
- Output ports of error statistics (input and output errors)
- Encoding delay is 8164 cycles (48.879 us)
- Decoding delay of 13 (7 horiz + 6 slope) decoding iterations is 16326 cycles (97.5667 us)

IP Core Parameters

Table 3 describes the I.9 BCH Encoder/Decoder IP Core parameters, which must be set before synthesis.

| Table 3. The I.9 BCH Encoder/Decoder IP Core parameters description |                               |
|---------------------------------------------------------------------|-------------------------------|
| Parameter                                                           | Description                   |
| ITER                                                                | number of decoding iterations |

For example:

- ITER = 5 means 5 decoding iterations totally:

idat - horiz1 - slope2 - horiz3 - slope4 - horiz5 - odat

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the I.9 BCH Encoder IP Core measurement results.

| Table 4. The I.9 BCH Encoder performance |                                                                     |                                       |                        |                        |
|------------------------------------------|---------------------------------------------------------------------|---------------------------------------|------------------------|------------------------|
| IP Core parameters                       | FPGA type                                                           |                                       |                        |                        |
|                                          | Resource                                                            | Speed grade, maximal system frequency |                        |                        |
| data width = 64 bit                      | Altera Stratix V 5SGSMD5                                            |                                       |                        |                        |
|                                          | 86478 ALMs (50%)<br>135 M20K RAM blocks (7%)<br>0 DSP (18x18) (0%)  | -4, Fmax                              | -3, Fmax               | -2, Fmax               |
|                                          |                                                                     | 170.0 MHz<br>10.8 Gbps                | 180.0 MHz<br>11.5 Gbps | 195.0 MHz<br>12.5 Gbps |
| data width = 64 bit                      | Xilinx Virtex-7 XC7VX485T                                           |                                       |                        |                        |
|                                          | 44376 Slices (59%)<br>146 18K RAM blocks (8%)<br>0 DSP (18x18) (0%) | -1, Fmax                              | -2, Fmax               | -3, Fmax               |
|                                          |                                                                     | 138.0 MHz<br>8.8 Gbps                 | 160.0 MHz<br>10.2 Gbps | 175.0 MHz<br>11.2 Gbps |

Table 5 summarizes the I.9 BCH Decoder IP Core measurement results.

| Table 5. The I.9 BCH Decoder performance |                                                                      |                                       |                        |          |
|------------------------------------------|----------------------------------------------------------------------|---------------------------------------|------------------------|----------|
| IP Core parameters                       | FPGA type                                                            |                                       |                        |          |
|                                          | Resource                                                             | Speed grade, maximal system frequency |                        |          |
| data width = 64 bit<br>13 iterations     | Altera Cyclone V 5CEFA7                                              |                                       |                        |          |
|                                          | 23900 ALMs (43%)<br>310 M10K RAM blocks (46%)<br>0 DSP (18x18) (0%)  | -8, Fmax                              | -7, Fmax               | -6, Fmax |
| 116.0 MHz<br>7.4 Gbps                    |                                                                      | 136.0 MHz<br>8.7 Gbps                 | 157.0 MHz<br>10.0 Gbps |          |
| data width = 64 bit<br>13 iterations     | Xilinx Virtex-7 XC7VX330T                                            |                                       |                        |          |
|                                          | 13429 Slices (27%)<br>251 18K RAM blocks (17%)<br>0 DSP (18x18) (0%) | -1, Fmax                              | -2, Fmax               | -3, Fmax |
| 219.0 MHz<br>14.0 Gbps                   |                                                                      | 244.0 MHz<br>15.6 Gbps                | 267.0 MHz<br>17.1 Gbps |          |

IP Core Interface Description

The encoder recognizes the first information symbol by the **isop** "start of information block" marker of that symbol (FAS OH = 0xF6F6F6282828). The bit width of input data **idat** and output data **odat** is 64 bits. The codec throughput of 10.7 Gbps requires a timing frequency of at least 170 MHz. The resulting encoded block at the encoder output can be recognized by the **osop** "start of encoded block" marker.

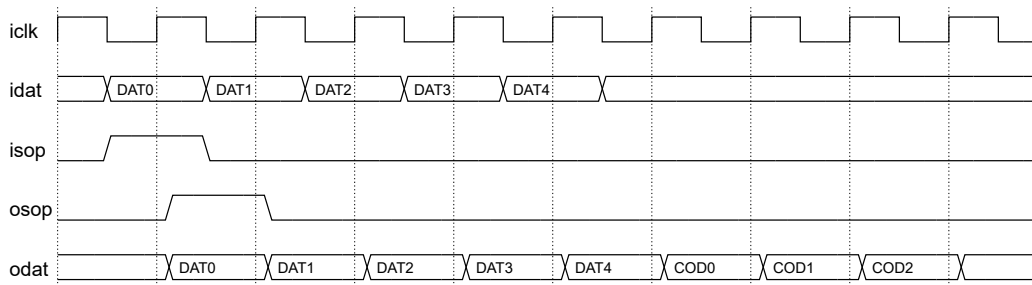


Figure 5. The timing diagrams of the I.9 BCH Encoder operation



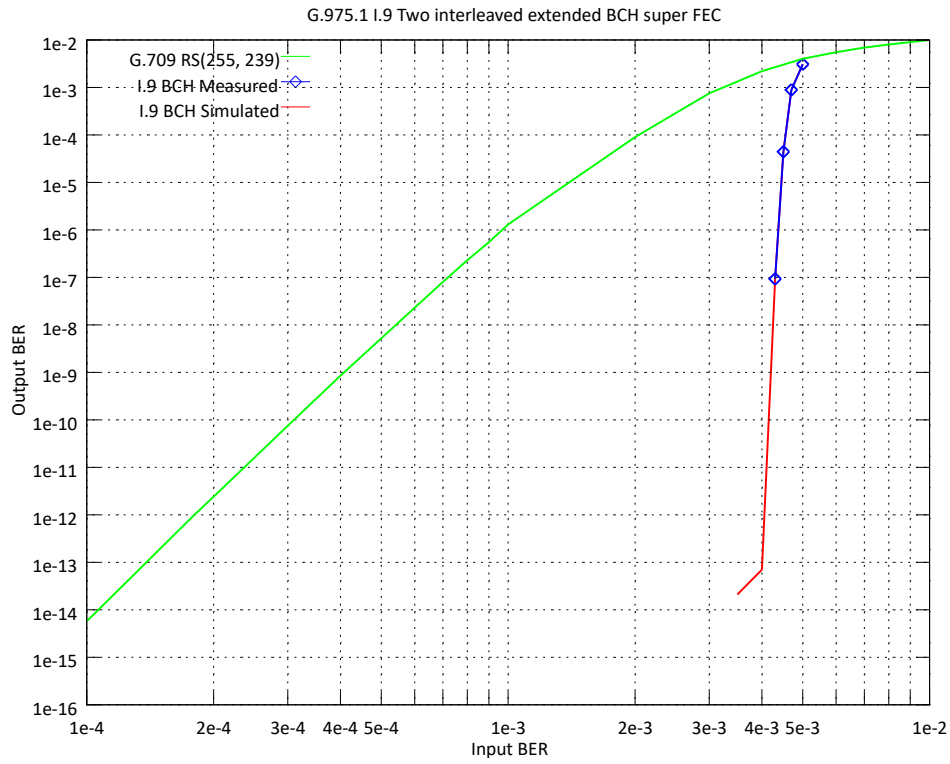


Figure 6. The error-correcting capability of the I.9 BCH Decoder

## Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

<https://www.iprium.com/ipcores/id/i9-bch-codec/>

## Feedback

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## Revision history

| Version | Date       | Changes                                                                                                  |
|---------|------------|----------------------------------------------------------------------------------------------------------|
| 2.1     | 2015.05.21 | Improved Encoder and Decoder performance                                                                 |
| 2.0     | 2014.09.23 | Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5 |
| 1.0     | 2013.04.02 | Official release                                                                                         |