IPRIUM

J.83 annex B Modulator IP Core Specification

Release Information

Name	J.83 annex B Modulator IP Core
Version	1.0
Build date	2019.08
Ordering code	ip-j83b-modulator
Specification revision	r1490

Features

The IP core is full-featured digital J83B modulator and is fully compatible with this standard:

- ITU-T J.83 annex B (12/2007)

Deliverables

The J.83 annex B Modulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the J.83 annex B Modulator IP Core block diagram.

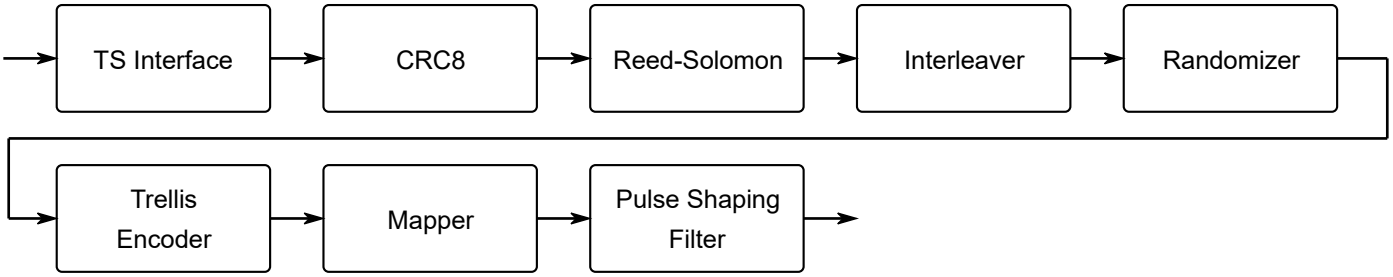

Figure 1. The J.83 annex B Modulator IP Core block diagram

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the J.83 annex B Modulator IP Core.

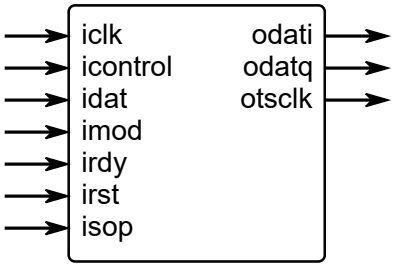

Figure 2. The J.83 annex B Modulator port map

Table 1. The J.83 annex B Modulator port map description		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
icontrol	4	Level 2 Interleaving control word: 0 - I=128, J=1 1 - I=128, J=1 2 - I=128, J=2 3 - I=64, J=2 4 - I=128, J=3 5 - I=32, J=4 6 - I=128, J=4 7 - I=16, J=8 8 - I=128, J=5 9 - I=8, J=16 10 - I=128, J=6 11 - Reserved 12 - I=128, J=7 13 - Reserved 14 - I=128, J=8 15 - Reserved
idat	8	input (information) data
imod	1	Modulation type: 0 - 64-QAM 1 - 256-QAM
irdy	1	Modulator output data request.
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	input sync-word byte marker (0x47 TS)
odati	W_DAC	modulator output at baseband (I channel) or at an intermediate frequency
odatq	W_DAC	modulator output at baseband (Q channel)
otsclk	1	ready to accept input data

IP Core Parameters

Table 2 describes the J.83 annex B Modulator IP Core parameters, which must be set before synthesis.

Table 2. The J.83 annex B Modulator IP Core parameters description	
Parameter	Description
W_DAC	Width of output DAC symbols (**odati/odatq**) Increasing the width of odati/odatq, increases the quality of waveform but also increases FPGA required resource

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the J.83 annex B Modulator IP Core measurement results.

Table 3. The J.83 annex B Modulator performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_DAC=16	Altera Cyclone 10 LP 10CL080			
	6620 LEs (8%) 56 M9K RAM blocks (18%) 0 DSP (18x18) (0%)	-8, Fmax	-7, Fmax	-6, Fmax
		100.0 MHz	120.0 MHz	140.0 MHz
W_DAC=16	Xilinx Virtex-7 XC7VX330T			
	1414 Slices (3%) 28 18K RAM blocks (2%) 0 DSP (18x18) (0%)	-1, Fmax	-2, Fmax	-3, Fmax
		180.0 MHz	220.0 MHz	260.0 MHz

IP Core Interface Description

IP core has two ways of forming the output spectrum:

- Baseband (using **odati** and **odatq**), **ifreq** equal 0
- Intermediate frequency (using **odati**), **ifreq** not equal 0

Digital-to-analog converters must operate synchronously with the J.83 annex B Modulator IP core. Figure 3 shows the DAC connection diagram for baseband mode and Figure 4 shows the timing diagram for this mode.

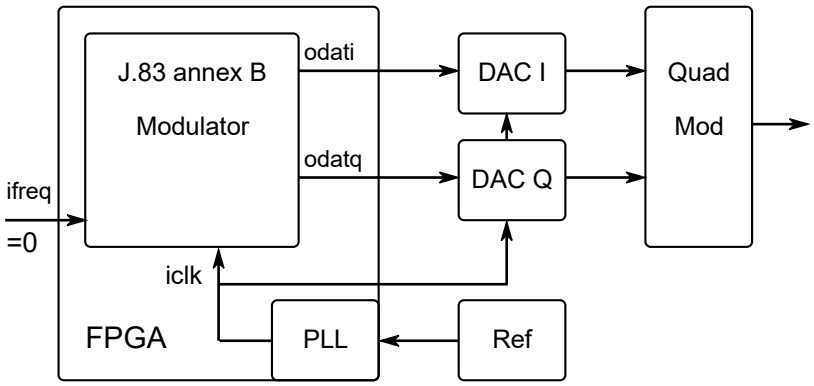

Figure 3. The DAC connection diagram for baseband mode.

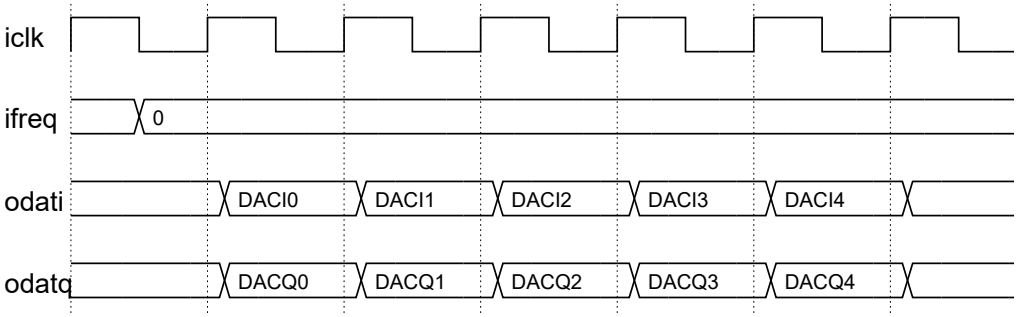

Figure 4. The timing diagram for baseband mode.

Figure 5 shows the DAC connection diagram for IF mode and Figure 6 shows the timing diagram for this mode. The output intermediate frequency port **ifreq** sets the central frequency for **odati** modulator output port.

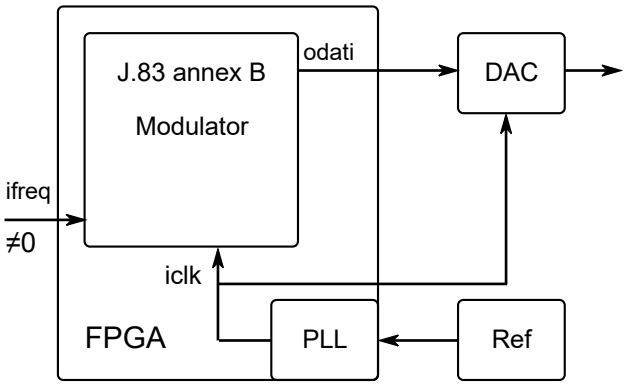

Figure 5. The DAC connection diagram for IF mode.

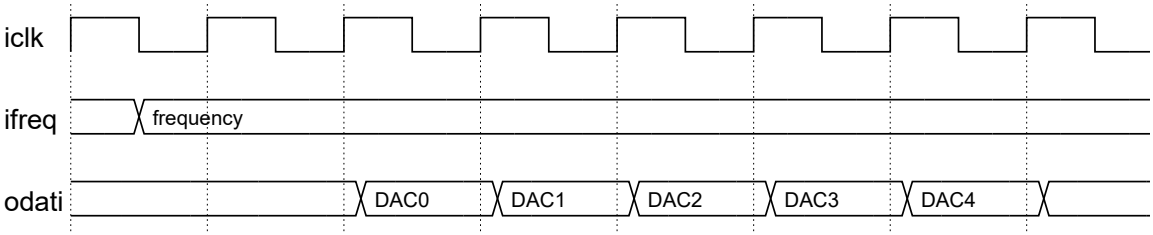

Figure 6. The timing diagram for IF mode.

Figure 7 shows an example of the waveform of the input interface. Handshake port **otsclk** controls input dataflow. Input data is read from the input **idat** only when **otsclk** is equal to logical one ("1").

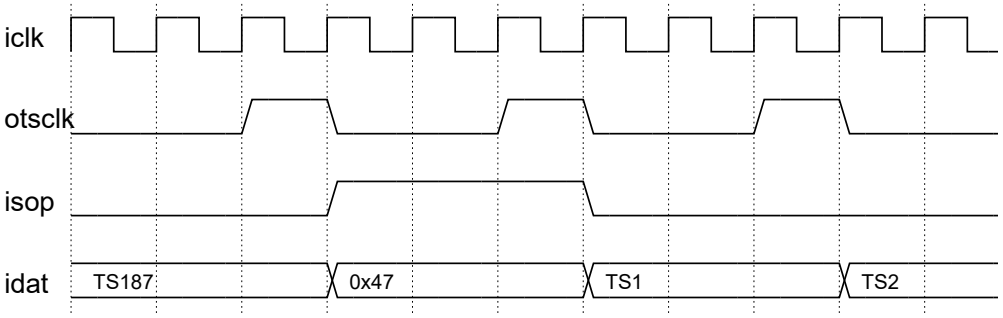

Figure 7. The timing diagram of the IP Core input interface.

The J.83 annex B Modulator IP Core supports 4-channel operating mode with the AD9789 RF DAC and allows to output spectrum 0 MHz to 1100 MHz.

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/j83b-modulator/

Feedback

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Revision history

Version	Date	Changes
1.0	2019.08.06	Official release