



J.83 annex B Modulator IP Core  
Specification

### Release Information

Name	J.83 annex B Modulator IP Core
Version	2.0
Build date	2021.06
Ordering code	ip-j83b-modulator
Specification revision	r1779

### Features

The IP core is full-featured 32-channel digital J.83 annex B modulator and is fully compatible with the standard:

- ITU-T J.83 annex B (12/2007)

### Price and License

Price:

- Netlist price : 4700 EUR
- Source code price : 28500 EUR
- +10% of the cost for each additional FPGA family netlist
- Customization price is 1000-5000 EUR

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

### Deliverables

The J.83 annex B Modulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

### IP Core Structure

Figure 1 shows the J.83 annex B Modulator IP Core block diagram for one channel.

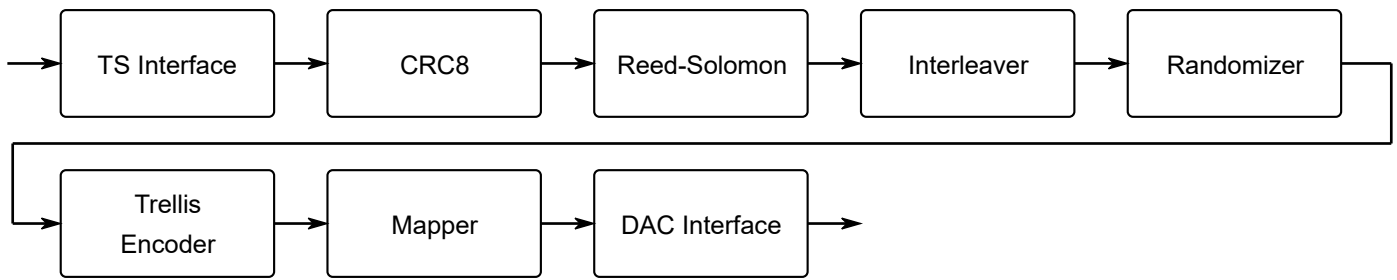


Figure 1. The J.83 annex B Modulator IP Core block diagram

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the J.83 annex B Modulator IP Core.

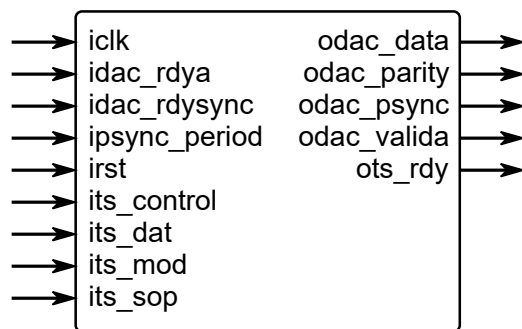


Figure 2. The J.83 annex B Modulator port map

Table 1. The J.83 annex B Modulator port map description		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idac_rdy	2	The RDYA signal from the DAC. Two bits are {second in time, first in time} IDDR outputs.
idac_rdy_sync	2	The RDYSYNC signal from the DAC. Two bits are {second in time, first in time} IDDR outputs.
ipsync_period	8	Number of timeslots of the DAC.
rst	1	The IP Core synchronously reset when rst is asserted high.

its_control	4	Level 2 Interleaving control word: 0 - I=128, J=1 1 - I=128, J=1 2 - I=128, J=2 3 - I=64, J=2 4 - I=128, J=3 5 - I=32, J=4 6 - I=128, J=4 7 - I=16, J=8 8 - I=128, J=5 9 - I=8, J=16 10 - I=128, J=6 11 - Reserved 12 - I=128, J=7 13 - Reserved 14 - I=128, J=8 15 - Reserved
its_dat	256	TS data for 32 parallel J.83B channels (1 channel = 8 bits).
its_mod	1	Modulation type for all channels: 0 - 64-QAM 1 - 256-QAM
its_sop	32	Input sync-word byte markers (0x47 TS) for 32 parallel J.83 annex B channels.
odac_data	20	The DAC DATA (constellation symbols) for ten parallel ODDR primitives.
odac_parity	2	The DAC PARITY data. Two bits are {second in time, first in time} ODDR inputs.
odac_psync	2	The DAC PSYNC data. Two bits are {second in time, first in time} ODDR inputs.
odac_valida	2	The DAC VALIDA data. Two bits are {second in time, first in time} ODDR inputs.
ots_rdy	32	Ready to accept TS data for 32 parallel J.83 annex B channels.

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 2 summarizes the J.83 annex B Modulator IP Core measurement results.

Table 2. The J.83 annex B Modulator performance		
IP Core parameters	FPGA type	
	Resource	Performance
MAX_TS = 32	Xilinx ZCU102 board, XCZU9EG	
	17809 CLBs (52%) 480 36K RAM blocks (53%) 0 DSP (18x18) (0%)	128+ MHz System Clock 32 J.83 annex B channels 64-QAM or 256-QAM

IP Core Interface Description

The J.83 annex B Modulator IP Core supports 32-channel operating mode with the MAX5861/MAX5862 DAC and allows to output spectrum 0 MHz to 1100 MHz.

Figure 3 shows the DAC connection diagram.

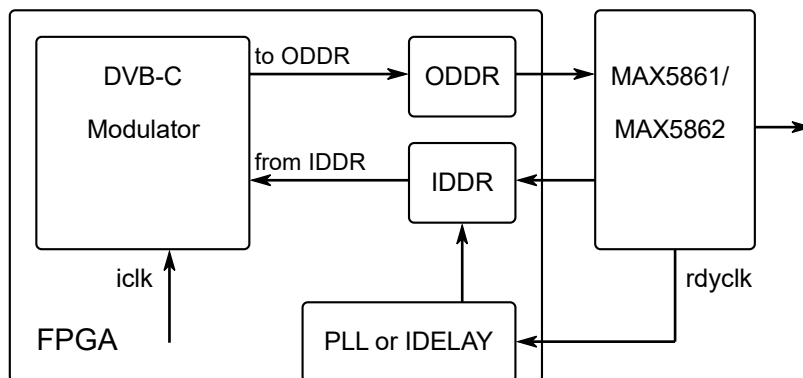
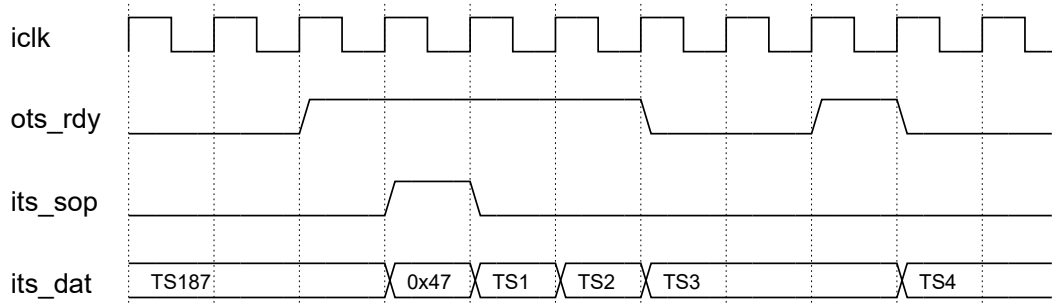


Figure 3. The connection diagram for MAX5861/MAX5862 DAC.

Figure 4 shows an example of the waveform of the input interface. Handshake port `ots_rdy` controls input dataflow. Input data is read from the input `its_dat` only when `ots_rdy` is equal to logical one ("1").



**Figure 4. The timing diagram of the IP Core input interface.**

### Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

<https://www.iprium.com/ipcores/id/j83b-modulator/>

### Feedback

IPrium LLC

39, via Umberto I, Ischitella (FG), 71010, Italy

Tel.: +39-375-6429155

E-mail: [info@iprium.com](mailto:info@iprium.com)

Skype: fpgahelp

website: <https://www.iprium.com/contacts/>

### Revision history

Version	Date	Changes
2.0	2021.06.01	32-channel J.83B modulator for MAX5861 and MAX5862 DAC
1.0	2019.08.06	Official release