LDPC NASA Encoder/Decoder IP Core Specification

Release Information

Name	LDPC NASA Codec IP Core
Version	2.0
Build date	2014.09
Ordering code	ip-ldpc-nasa-codec
Specification revision	r1383

Features

The IP core implements the LDPC NASA CCSDS C2 (8176, 7154) forward error correction algorithm and is fully compatible with standard:

- GSFC-STD-9100 (Low Density Parity Check Code for Rate 7/8)

Deliverables

The LDPC NASA Encoder/Decoder IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the LDPC NASA Encoder IP Core block diagram.

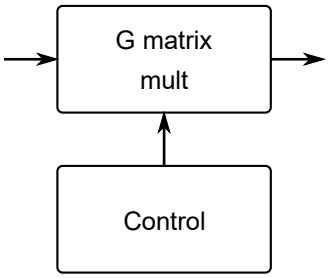

Figure 1. The LDPC NASA Encoder IP Core block diagram

The LDPC NASA Encoder consists of a control module (**Control**) and a generator matrix multiplier module (**G matrix mult**).

Figure 2 shows the LDPC NASA Decoder IP Core block diagram.

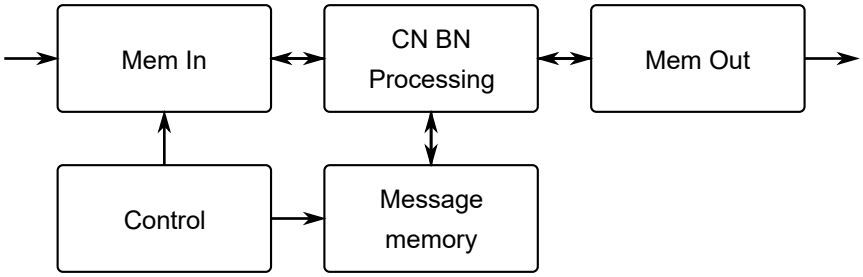

Figure 2. The LDPC NASA Decoder IP Core block diagram

The LDPC NASA Decoder consists of a control module (**Control**), input memory buffer (**Mem In**), an output memory buffer (**Mem Out**), a message memory (**Message Memory**) and a LLR processing module (**CN BN Processing**).

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the LDPC NASA Encoder IP Core.

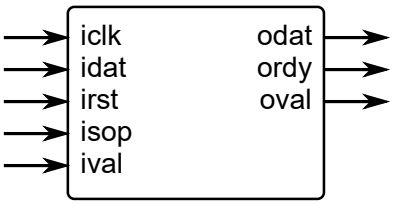

Figure 3. The LDPC NASA Encoder port map

Table 1. The LDPC NASA Encoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	1	input (information) data
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of information packet marker
ival	1	input data valid
odat	1	output (encoded) data
ordy	1	ready to accept input data
oval	1	output data valid

Figure 4 shows a graphic symbol, and Table 2 gives a description of the LDPC NASA Decoder IP Core ports.

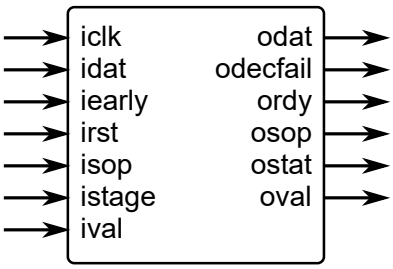

Figure 4. The LDPC NASA Decoder port map

Table 2. The LDPC NASA Decoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	W_IN	input (encoded) LLR data
iearly	1	enable "early stop detection"
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	start of coded packet marker
istage	W_STAGE	number of decoding iterations
ival	1	input data valid
odat	1	output (decoded) data
odecfail	1	failed to decode flag
ordy	1	ready to accept input data
osop	1	start of decoded packet marker
ostat	2	status of encoded packet: 0 - no data output 1 - infomation data output 2 - parity data output
oval	1	output data valid

IP Core Parameters

Table 3 describes the LDPC NASA Encoder/Decoder IP Core parameters, which must be set before synthesis.

Table 3. The LDPC NASA Encoder/Decoder IP Core parameters description

Parameter	Description

W_IN	Width of decoder LLR input symbol (**idat**). Increasing the width of idat, increases the accuracy of the LLR value but also increases FPGA required resource
W_LLR	Width of internal LLR accumulators. Increasing the width of LLR accumulators, increases the precision of the decoding but also increases FPGA required resource
W_STAGE	Maximum number of decoding iterations (**istage**). Increasing the number of iterations, increases the quality of decoding but laso decrease decoder throughput

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the LDPC NASA Encoder IP Core measurement results.

Table 4. The LDPC NASA Encoder performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_IN=1	Altera Cyclone IV EP4CE75			
	2,158 LEs 0 M9K RAM blocks 0 DSP (18x18)	-8, Fmax	-7, Fmax	-6, Fmax
		230.0 MHz 230.0 Mbit/s	269.0 MHz 269.0 Mbit/s	318.0 MHz 318.0 Mbit/s
W_IN=1	Xilinx Virtex-6 XC6VLX240T			
	290 Slices 0 18K RAM blocks 0 DSP (18x18)	-1, Fmax	-2, Fmax	-3, Fmax
		418.0 MHz 418.0 Mbit/s	490.0 MHz 490.0 Mbit/s	570.0 MHz 570.0 Mbit/s

Table 5 summarizes the LDPC NASA Decoder IP Core measurement results.

Table 5. The LDPC NASA Decoder performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_IN=6 W_LLR=9 W_STAGE=5 8 stages of decoding	Altera Cyclone IV EP4CE75			
	4,139 LEs 44 M9K RAM blocks 0 DSP (18x18)	-8, Fmax	-7, Fmax	-6, Fmax
		156.0 MHz 48.6 Mbit/s	182.7 MHz 56.9 Mbit/s	203.8 MHz 63.5 Mbit/s
W_IN=6 W_LLR=9 W_STAGE=5 8 stages of decoding	Xilinx Virtex-6 XC6VLX240T			
	1,088 Slices 22 18K RAM blocks 0 DSP (18x18)	-1, Fmax	-2, Fmax	-3, Fmax
		240.0 MHz 74.7 Mbit/s	271.0 MHz 84.4 Mbit/s	298.0 MHz 92.8 Mbit/s

IP Core Interface Description

The encoder and decoder recognize the first information symbol by the **isop** "start of information block" marker. The resulting encoded/decoded block at the encoder/decoder output can be recognized by the **osop** "start of encoded block" marker. Additionally the encoder marks the status of the output data by **ostat**:

- 0 - no data output
- 1 - information symbols of encoded block
- 2 - parity (check) symbols of encoded block

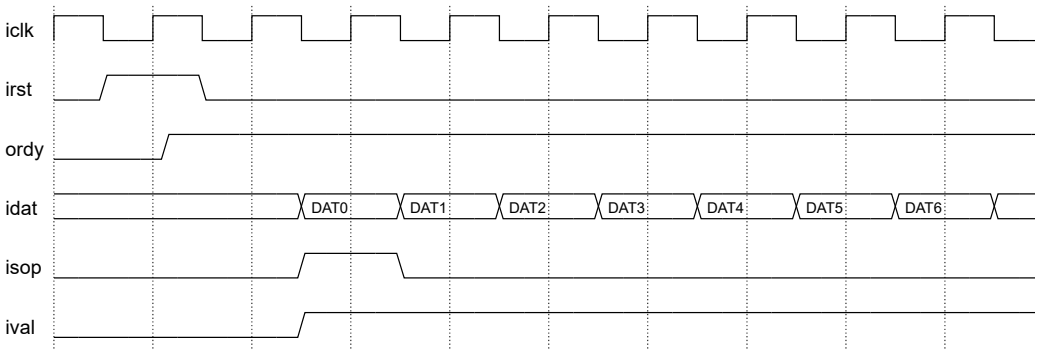

Figure 5. The timing diagrams of the LDPC NASA Decoder operation (input)

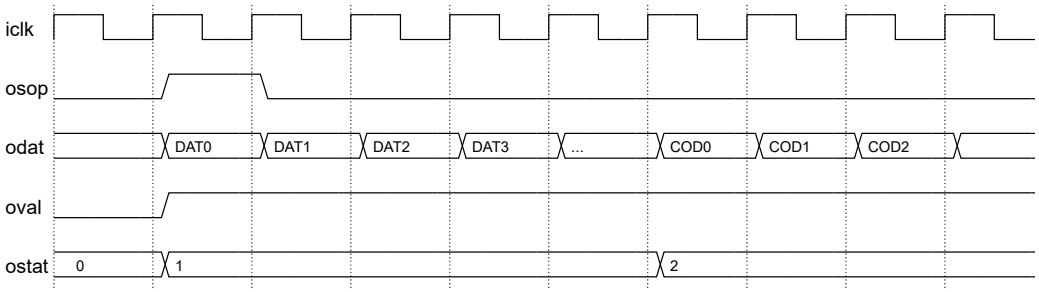

Figure 6. The timing diagrams of the LDPC NASA Decoder operation (output)

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/ldpc-nasa-codec/

Feedback

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Revision history

Version	Date	Changes
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.1	2013.01.18	Improve decoder performance
1.0	2012.04.04	Official release