OFDM Modulator/Demodulator IP Core Specification

Release Information

Name	OFDM Modem IP Core
Version	2.0
Build date	2014.09
Ordering code	ip-ofdm-modem
Specification revision	r1465

Features

The IP core implements the OFDM modulation/demodulation algorithm with differential PSK subcarrier modulation (DBPSK, DQPSK, D8PSK).

Deliverables

The OFDM Modulator/Demodulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the OFDM Modulator/Demodulator IP Core block diagram.

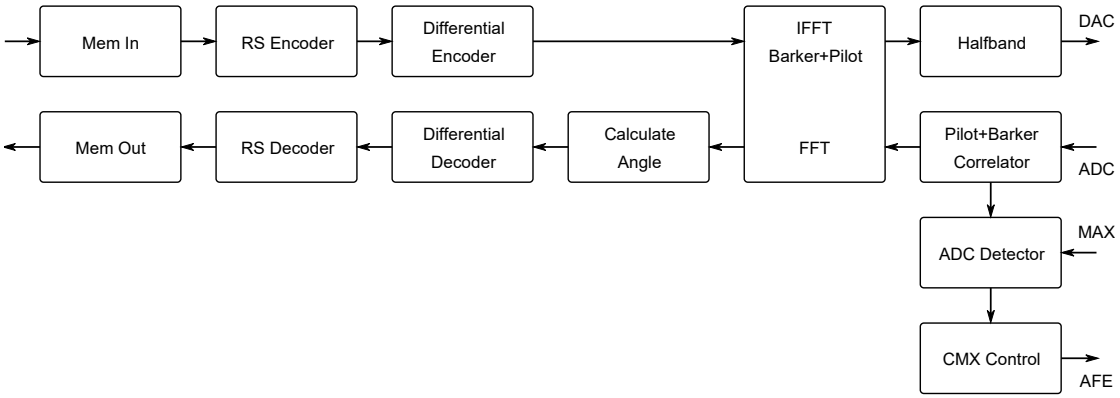

Figure 1. The OFDM Modem IP Core block diagram

The OFDM modem consists of input and output memory buffers (**Mem In**, **Mem Out**), Reed-Solomon encoder/decoder (**RS Encoder**, **RS Decoder**), a differential decoder/PSK demapper (**Differential Decoder**), I and Q complex channel values to polar coordinates "angle / amplitude" conversion module (**Calculate Angle**), a Fast Fourier Transform engine module (**IFFT/FFT**), a Low-pass filter (**Halfband**) and an AGC control module (**ADC Detector**, **CMX Control**).

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the OFDM Modulator/Demodulator IP Core.

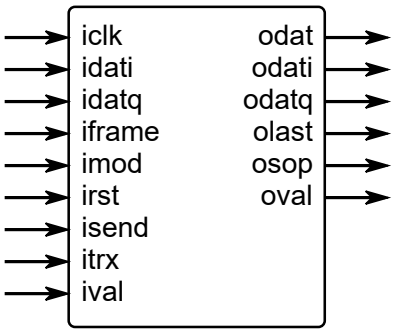

Figure 2. The OFDM Modulator/Demodulator port map

Table 1. The OFDM Modulator/Demodulator port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idati	W_IN	ADC I channel
idatq	W_IN	ADC Q channel
iframe	9	number of FFT symbols in frame
imod	2	subcarrier modulation type: 0 - DBPSK 1 - DQPSK 2 - D8PSK
irst	1	The IP Core synchronously reset when irst is asserted high.
isend	1	data send command
itrx	1	modem work mode: 0 - RX (receiver) 1 - TX (transmitter)
ival	1	ADC input data valid
odat	8	dmodulator output data (for RS Decoder)
odati	W_DAC	DAC I channel (after Halfband).
odatq	W_DAC	DAC Q channel (after Halfband).
olast	1	last output symbol marker

osop	1	start of output data marker for RS Decoder
oval	1	output data valid for RS Decoder

IP Core Parameters

Table 2 describes the OFDM Modulator/Demodulator IP Core parameters, which must be set before synthesis.

Table 2. The OFDM Modulator/Demodulator IP Core parameters description

Parameter	Description
GUARD	Number of FFT points in gaurd interval.
PREAMB	Preamble/Pilot length.
W_IN	ADC width (**idati**, **idatq**).
W_DAC	DAC width (**odati**, **odatq**).

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the OFDM Modem IP Core measurement results.

Table 4. The OFDM Modem performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
GUARD=16 PREAMB=3000 W_IN=10 W_DAC=10 FFT 256 points	Altera Cyclone IV EP4CE75			
	4,139 LEs 44 M9K RAM blocks 0 DSP (18x18)	-8, Fmax	-7, Fmax	-6, Fmax
		156.0 MHz 48.6 Mbit/s	182.7 MHz 56.9 Mbit/s	203.8 MHz 63.5 Mbit/s
GUARD=16 PREAMB=3000 W_IN=10 W_DAC=10 FFT 256 points	Xilinx Virtex-6 XC6VLX240T			
	1,088 Slices 22 18K RAM blocks 0 DSP (18x18)	-1, Fmax	-2, Fmax	-3, Fmax
		240.0 MHz 74.7 Mbit/s	271.0 MHz 84.4 Mbit/s	298.0 MHz 92.8 Mbit/s

IP Core Interface Description

The encoder and decoder recognize the first information symbol by the **isop** "start of information block" marker. The resulting encoded/decoded block at the encoder/decoder output can be recognized by the **osop** "start of encoded block" marker. Additionally the encoder marks the status of the output data by **ostat**:

- 0 - no data output
- 1 - information symbols of encoded block
- 2 - parity (check) symbols of encoded block

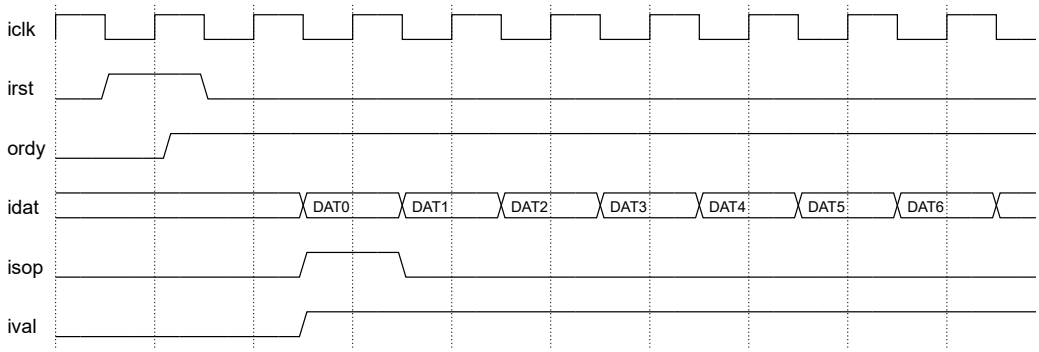

Figure 3. The timing diagrams of the OFDM demodulator operation (input)

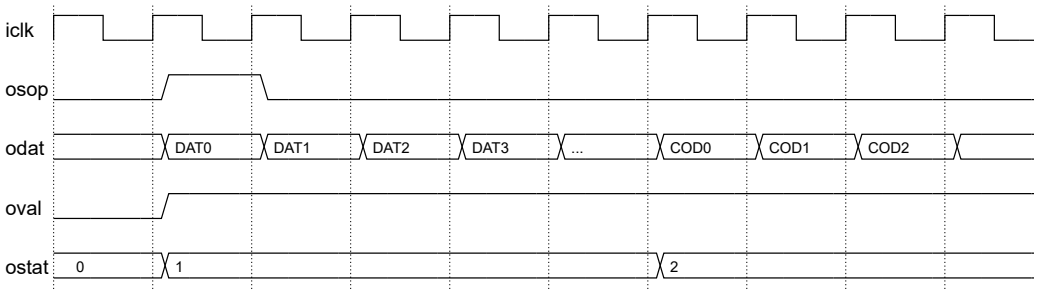

Figure 4. The timing diagrams of the OFDM demodulator operation (output)

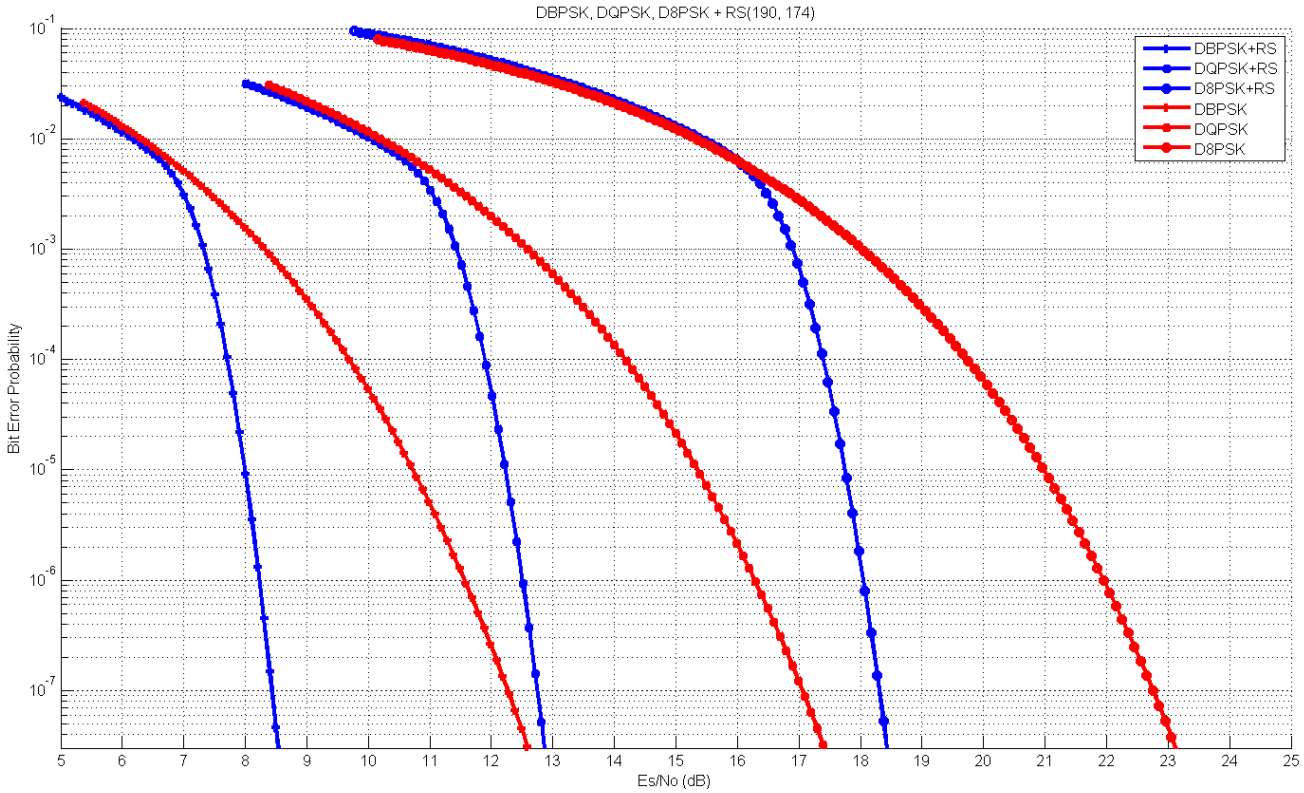

Figure 5. The OFDM Modem performance in AWGN channel

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/ofdm-modem/

Feedback

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Revision history

Version	Date	Changes
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.1	2013.03.19	Improve modem performance
1.0	2012.09.04	Official release