PSK Demodulator IP Core Specification

Release Information

Name	PSK Demodulator IP Core
Version	2.0
Build date	2017.11
Ordering code	ip-psk-demodulator
Specification revision	r1383

Features

The IP core is full-featured digital PSK demodulator.

Deliverables

The PSK Demodulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the PSK Demodulator IP Core block diagram.

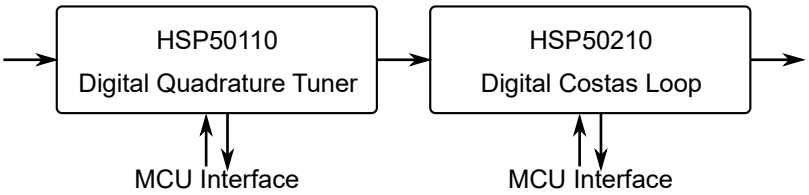

Figure 1. The PSK Demodulator IP Core block diagram

The PSK Demodulator consists of a **HSP50110** (Digital Quadrature Tuner) and a **HSP50210** (Digital Costas Loop). The IP Core is fully compatible with HSP50110 and HSP50210 ICs and is exact FPGA replacement.

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the PSK Demodulator IP Core.

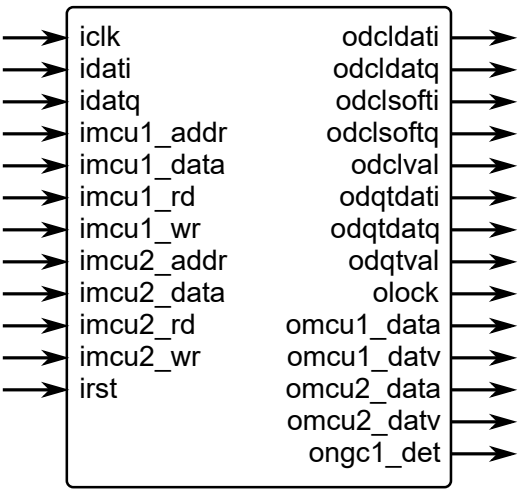

Figure 2. The PSK Demodulator port map

Table 1. The PSK Demodulator port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idati idatq	10	ADC samples for demodulation.
imcu1_addr	3	HSP50110 MCU address
imcu1_data	8	HSP50110 MCU data
imcu1_rd	1	HSP50110 MCU read signal
imcu1_wr	1	HSP50110 MCU write signal
imcu2_addr	3	HSP50210 MCU address
imcu2_data	8	HSP50210 MCU data
imcu2_rd	1	HSP50210 MCU read signal
imcu2_wr	1	HSP50210 MCU write signal
irst	1	The IP Core synchronously reset when irst is asserted high.
odcldati, odcldatq	8	HSP50210 output constellation
odclsofti, odclsofti	3	HSP50210 soft decision
odclval	1	HSP50210 output valid signal

odqtdati, odqtdatq	10	HSP50110 output data
odqtval	1	HSP50110 output valid signal
olock	1	Lock detector signal
imcu1_data	8	HSP50110 MCU data
imcu1_datv	1	HSP50110 MCU read/write select signal
imcu2_data	8	HSP50210 MCU data
imcu2_datv	1	HSP50210 MCU read/write select signal
ongc1_det	1	Input AGC detector signal

IP Core Parameters

Table 2 describes the PSK Demodulator IP Core parameters, which must be set before synthesis.

Table 2. The PSK Demodulator IP Core parameters description

Parameter	Description
There are no parameters available to change	

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the PSK Demodulator IP Core measurement results.

Table 3. The PSK Demodulator performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
	Altera Cyclone V 5CEFA7			
	4193 ALMs (8%) 2 M10K RAM blocks (1%) 8 DSP (18x18) (6%)	-8, Fmax	-7, Fmax	-6, Fmax
		78.0 MHz 39.0 Msymb/s	90.0 MHz 45.0 Msymb/s	102.0 MHz 51.0 Msymb/s
	Xilinx Virtex-7 XC7VX330T			
	2588 Slices (6%) 2 18K RAM blocks (1%) 12 DSP (18x18) (1%)	-1, Fmax	-2, Fmax	-3, Fmax
		124.0 MHz 62.0 Msymb/s	170.0 MHz 85.0 Msymb/s	190.0 MHz 95.0 Msymb/s

IP Core Interface Description

Description of the interface can be found in the original HSP50110 and HSP50210 user guide from the Intersil (Harris) company.

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/psk-demodulator/

Feedback

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Revision history

Version	Date	Changes
2.0	2017.11.14	Added CPU interface
1.0	2014.10.14	Official release