IPRIUM

# QAM Modulator IP Core Specification

## Release Information

| | |
|---|---|
| Name | QAM Modulator IP Core |
| Version | 4.0 |
| Build date | 2014.09 |
| Ordering code | ip-qam-modulator |
| Specification revision | r1908 |

## Features

The IP core implements the full-featured QAM modulation algorithm and is fully compatible with those standards:

- Digital Video Broadcasting (DVB-S, DVB-C, DVB-S2, DVB-S2X)
- Satellite Broadcasting
- ITU-T for point-to-point microwave communication systems

## License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

## Deliverables

The QAM Modulator IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

## IP Core Structure

Figure 1 shows the QAM Modulator IP Core block diagram.

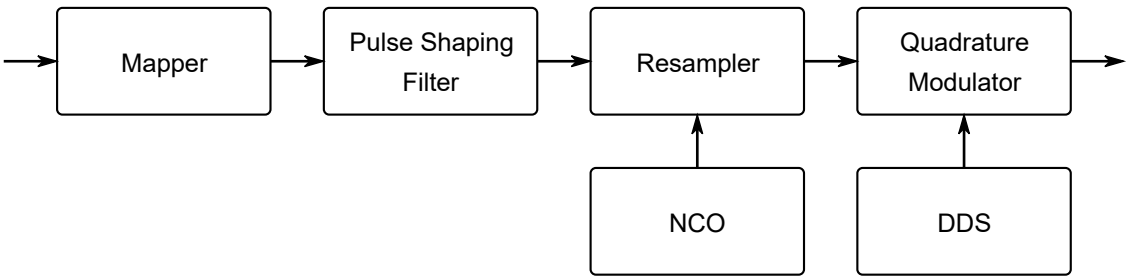


**Figure 1. The QAM Modulator IP Core block diagram**

The QAM modulator consists of a constellation mapper (**Mapper**), a RRC filter (**Pulse Shaping Filter**), a fractional

resampler/interpolator (**Resampler**), a quadrature modulator (**Quadrature Modulator**), a numerically controlled oscillator (**NCO**) and a direct digital synthesis module (**Direct Digital Synthesis**).

## Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the QAM Modulator IP Core.

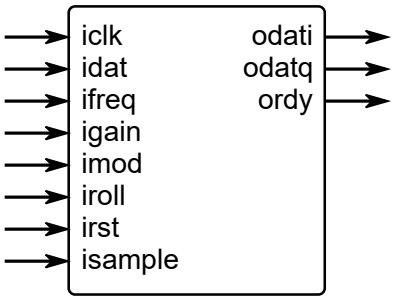


**Figure 2. The QAM Modulator port map**

**Table 1. The QAM Modulator port map description**

| Port | Width | Description |
|---|---|---|
| iclk | 1 | The main system clock. The IP Core operates on the rising edge of iclk. |
| idat | | input (information) data |
| ifreq | 32 | output intermediate frequency |
| igain | W_DAC | output gain control |
| imod | | modulation:<br>specified before IP Core order |
| iroll | | RRC filter roll-off factor |
| irst | 1 | The IP Core synchronously reset when irst is asserted high. |
| isample | 32 | bandwidth control (symbol rate):<br>0.01% to 25% of iclk |
| odati | W_DAC | modulator output at baseband (I channel) or at an intermediate frequency |
| odatq | W_DAC | modulator output at baseband (Q channel) |
| ordy | 1 | ready to accept input data |

## IP Core Parameters

Table 2 describes the QAM Modulator IP Core parameters, which must be set before synthesis.

**Table 2. The QAM Modulator IP Core parameters description**

| Parameter | Description |
|---|---|
| **W_DAC** | Width of output DAC symbols (**odati/odatq**)<br>Increasing the width of odati/odatq, increases the quality of waveform but also increases FPGA required resource |
| **CONFIG** | Set of mapping tables and QAM/APSK constellations.<br>IP Core supports BPSK, QPSK, 8-PSK, 16-APSK, 32-APSK, 64-APSK, 128-APSK, 256-APSK, 16-QAM, 32-QAM, 64-QAM, 128-QAM, 256-QAM, 512-QAM, 1024-QAM modulations.<br>For example, CONFIG="DVB-S2X" contains all DVB-S2 and DVB-S2X standard constellations. |
| **ROLL-OFF** | Set of roll-off factors (alpha) for shaping filter (RRC).<br>For example, ROLL-OFF = 0.35, 0.25, 0.20, 0.15, 0.10 Pë 0.05. |

## IP Core Operation Description

Quadrature Amplitude Modulation (QAM modulation) is the most efficient in the use of spectrum by the transmission of information. QAM modulated signal is the sum of two orthogonal subcarriers, each of which is modulated in amplitude. Total oscillation is obtained simultaneously modulated both in amplitude and phase. The number of levels of amplitude modulation in each subcarrier is fixed and determines the type of modulated signal constellations. When the number of modulation levels, increases the amount of information carried by each symbol QAM signal.

Key features of the IP Core:

- Synchronous, high-speed algorithm for the formation BPSK/QPSK/QAM/APSK signals
- The output of the intermediate frequency range up to 40% of the system clock frequency
- Symbol rate to 1/4 of the system clock frequency
- Support for changing modulation schemes "on the fly"
- Parameterized shaping filter and fractional interpolator
- Fixed delay in the modulator

## Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the QAM Modulator IP Core measurement results.

| Table 3. The QAM Modulator performance | | | | |
|---|---|---|---|---|
| **IP Core parameters** | **FPGA type** | | | |
| | **Resource** | **Speed grade, maximal system frequency** | | |
| W_DAC=16 CONFIG="DVB-S2X" ROLL-OFF=0.35, 0.25, 0.20, 0.15, 0.10, 0.05 | Altera Cyclone IV EP4CE75 | | | |
| | 15713 LEs<br>11 M9K RAM blocks<br>12 DSP (18x18) | -8, Fmax | -7, Fmax | -6, Fmax |
| | | 104.0 MHz<br>26.0 Msymb/s | 119.0 MHz<br>29.75 Msymb/s | 135.0 MHz<br>33.75 Msymb/s |
| W_DAC=16 CONFIG="DVB-S2X" ROLL-OFF=0.35, 0.25, 0.20, 0.15, 0.10, 0.05 | Xilinx Virtex-6 XC6VLX240T | | | |
| | 5125 Slices<br>10 18K RAM blocks<br>12 DSP (18x18) | -1, Fmax | -2, Fmax | -3, Fmax |
| | | 144.0 MHz<br>36.0 Msymb/s | 166.0 MHz<br>41.5 Msymb/s | 184.0 MHz<br>46.0 Msymb/s |

## IP Core Interface Description

IP core has two ways of forming the output spectrum:

- Baseband (using **odati** and **odatq**), **ifreq** equal 0
- Intermediate frequency (using **odati**), **ifreq** not equal 0

Digital-to-analog converters must operate synchronously with the QAM Modulator IP core. Figure 3 shows the DAC connection diagram for baseband mode and Figure 4 shows the timing diagram for this mode.

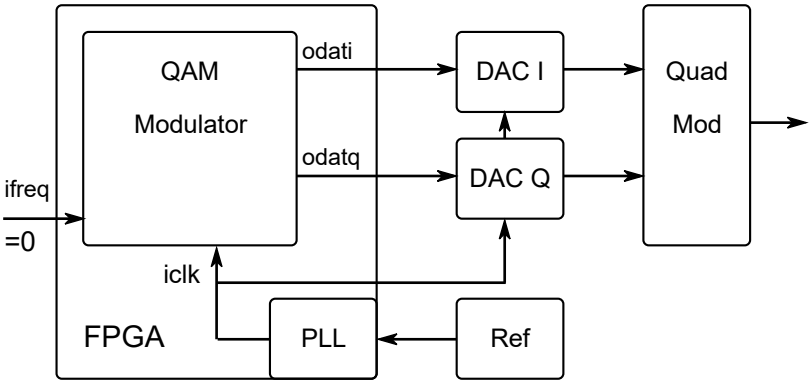


**Figure 3. The DAC connection diagram for baseband mode.**

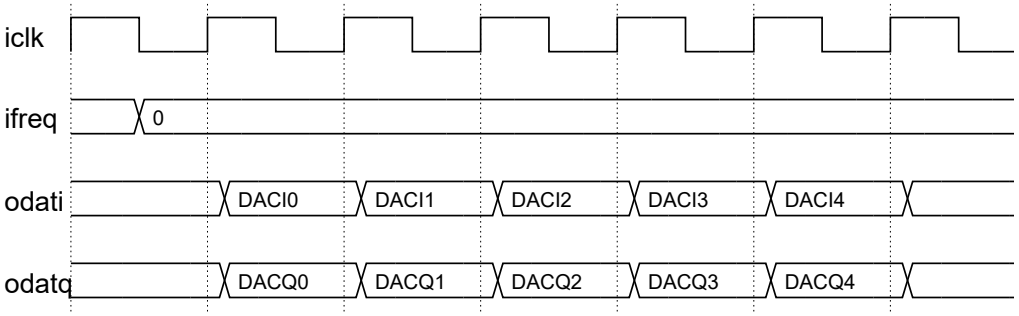


**Figure 4. The timing diagram for baseband mode.**

Figure 5 shows the DAC connection diagram for IF mode and Figure 6 shows the timing diagram for this mode. The output intermediate frequency port **ifreq** sets the central frequency for **odati** modulator output port.

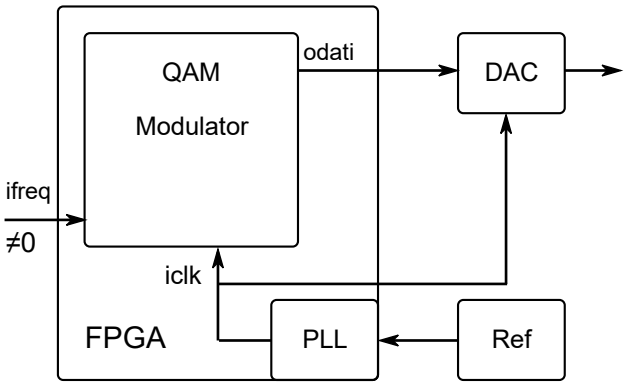


**Figure 5. The DAC connection diagram for IF mode.**

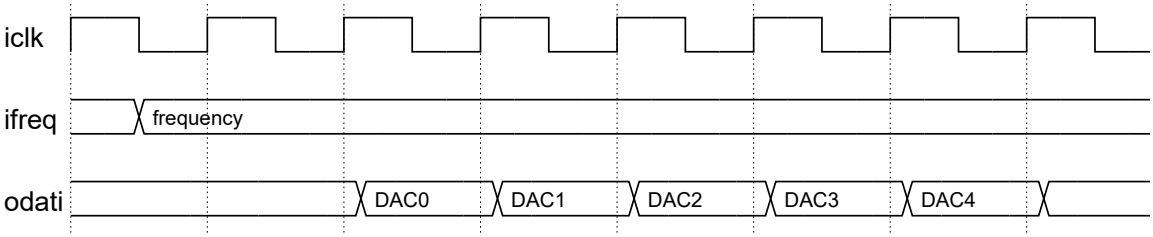


**Figure 6. The timing diagram for IF mode.**

Figure 7 shows an example of the waveform of the input interface. Handshake port **ordy** controls input dataflow. Input data is read from the input **idat** only when **ordy** is equal to logical one ("1").

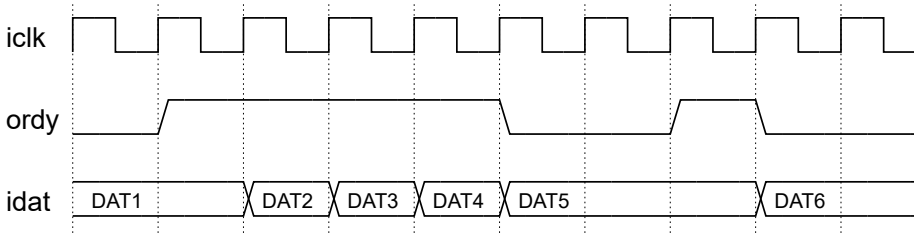


**Figure 7. The timing diagram of the IP Core input interface.**

## Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/qam-modulator/

## Feedback

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## Revision history

| Version | Date | Changes |
|---|---|---|
| 4.0 | 2014.09.23 | Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5 |
| 3.0 | 2014.03.25 | Added 128-APSK and 256-APSK modulation support |
| 2.1 | 2010.10.12 | Maintenance improvements |
| 2.0 | 2009.08.18 | Added 16-APSK/32-APSK/64-APSK modulation support |
| 1.2 | 2008.10.10 | Added 256-QAM/1024-QAM modulation support |
| 1.1 | 2008.06.04 | Added 64-QAM modulation support |
| 1.0 | 2007.03.06 | Official release |