IPRIUM

Reed-Solomon Encoder/Decoder IP core Specification

Release Information

Name	Reed-Solomon Codec IP core
Version	3.0
Build date	2016.04
Ordering code	ip-rs-codec
Specification revision	r1908

Features

The IP core implements the Reed-Solomon forward error correction algorithm and is fully compatible with those standards:

- Digital TV broadcasting (DVB-S, DVB-C, DVB-T)
- IEEE 802.11ad (WiGig, multi-gigabit wireless technology)
- IEEE 802.16 (WiMAX modems)
- ITU G.992.1 (ADSL modems)
- ITU-T G.975 (2.5G, 10G and 40G optical networks)
- CD-ROM, DVD, Compact Flash (data storage devices)

License

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The Reed-Solomon Encoder/Decoder IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the Reed-Solomon Encoder IP Core block diagram.

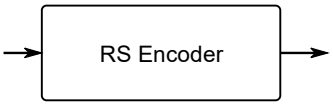

Figure 1. The Reed-Solomon Encoder IP Core block diagram

Figure 2 shows the Reed-Solomon Decoder IP Core block diagram.

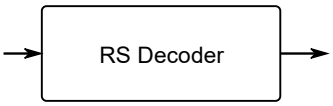

Figure 2. The Reed-Solomon Decoder IP Core block diagram

Port Map

Figure 3 shows a graphic symbol, and Table 1 describes the ports of the Reed-Solomon Encoder IP Core.

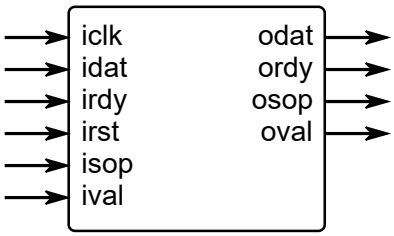

Figure 3. The Reed-Solomon Encoder port map

Table 1. The Reed-Solomon Encoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	8	Input information data.
irdy	1	Output encoded data request.
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	Start of block for input data.
ival	1	Input data valid.
odat	8	Encoded data output.
ordy	1	Ready to accept input data.
osop	1	Start of block for output encoded data.
oval	1	Ouptut encoded data valid.

Figure 4 shows a graphic symbol, and Table 2 describes the ports of the Reed-Solomon Decoder IP Core.

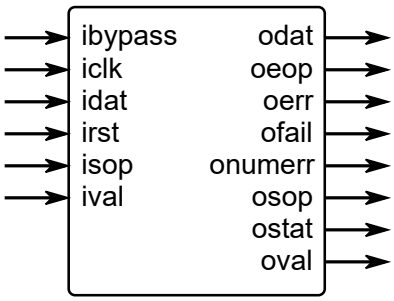

Figure 4. The Reed-Solomon Decoder port map

Table 2. The Reed-Solomon Decoder port map description

Port	Width	Description
ibypass	1	Bypass decoder and output uncorrected data.
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idat	8	Input encoded data.
irst	1	The IP Core synchronously reset when irst is asserted high.
isop	1	Start of block for input data.
ival	1	Input data valid.
odat	8	Decoded data output.
oeop	1	End of block for output decoded data.
oerr	1	Correction mask for output decoded data.
ofail	1	Decoder failed to correct errors in the current block. Number of errors exceeds decoder correction capability.
onumerr	W_ERR	Numer of corrected errors in the current block.
osop	1	Start of block for output decoded data.
ostat	2	Output decoded data status: 0 - no data 1 - information symbols 2 - coded symbols

oval	1	Ouptut decoded data valid.

IP Core Operation Description

Digital telecommunication systems use forward error correction techniques to avoid bit errors.

IP Core Parameters

Table 3 describes RS Encoder/Decoder IP Core parameters, which must be set before synthesis.

Table 3. RS Encoder/Decoder IP Core parameters description

Parameter	Description
M = 8	RS symbol width is always equal **8**.
K	Information block length.
N	Codeword block length.
W_ERR	Width of **onumerr** port, depends on **N-K**.

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the RS Encoder IP Core measurement results.

Table 4. RS Encoder performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
K = 188 N = 204 W_ERR = 5	Altera Cyclone II EP2C35			
	655 LEs 8,192 bits	-8, Fmax	-7, Fmax	-6, Fmax
		190.0 MHz 163.0 MHz (RAM limit)	247.0 MHz 195.0 MHz (RAM limit)	280.0 MHz 235.0 MHz (RAM limit)
K = 188 N = 204 W_ERR = 5	Xilinx Spartan-3A DSP XC3SD1800			
	329 slices 8,192 bits	-4, Fmax	-5, Fmax	
		184.0 MHz	210.0 MHz	

Table 5 summarizes the RS Decoder IP Core measurement results.

Table 5. RS Decoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
K = 188 N = 204 W_ERR = 5	Altera Cyclone II EP2C35			
	3,612 LEs 32,768 bits	-8, Fmax	-7, Fmax	-6, Fmax
		110.0 MHz	134.0 MHz	150.0 MHz
K = 188 N = 204 W_ERR = 5	Xilinx Spartan-3A DSP XC3SD1800			
	1,851 slices 32,768 bits	-4, Fmax	-5, Fmax	
		129.0 MHz	149.0 MHz	

IP Core Interface Description

The encoder recognizes the first information symbol by the **isop** "start of information block" marker. The resulting encoded block at the encoder output can be recognized by the **osop** "start of encoded block" marker. Additionally the encoder marks the status of the output data by **ostat**:

- 0 - no data output
- 1 - information symbols of encoded block
- 2 - parity (check) symbols of encoded block

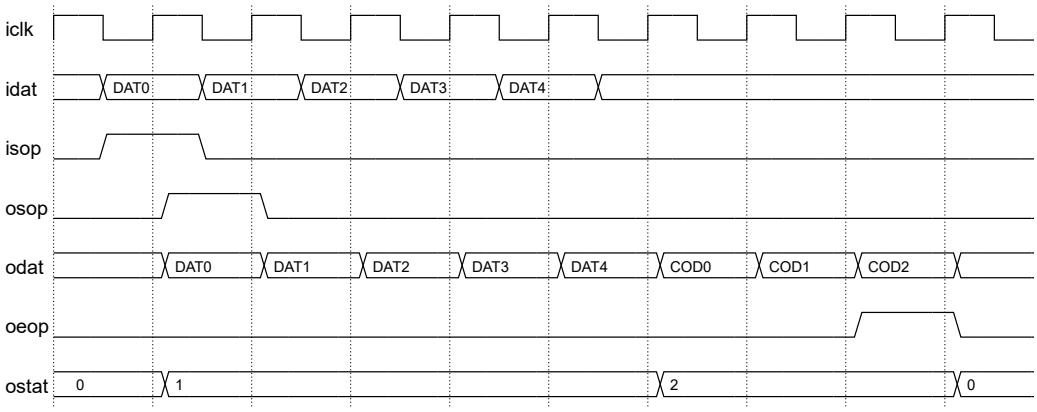

Figure 5. The timing diagrams of the Reed-Solomon Encoder operation

Quality Metrics

The error-correcting capability of the RS Decoder IP Core is shown on the figure 6.

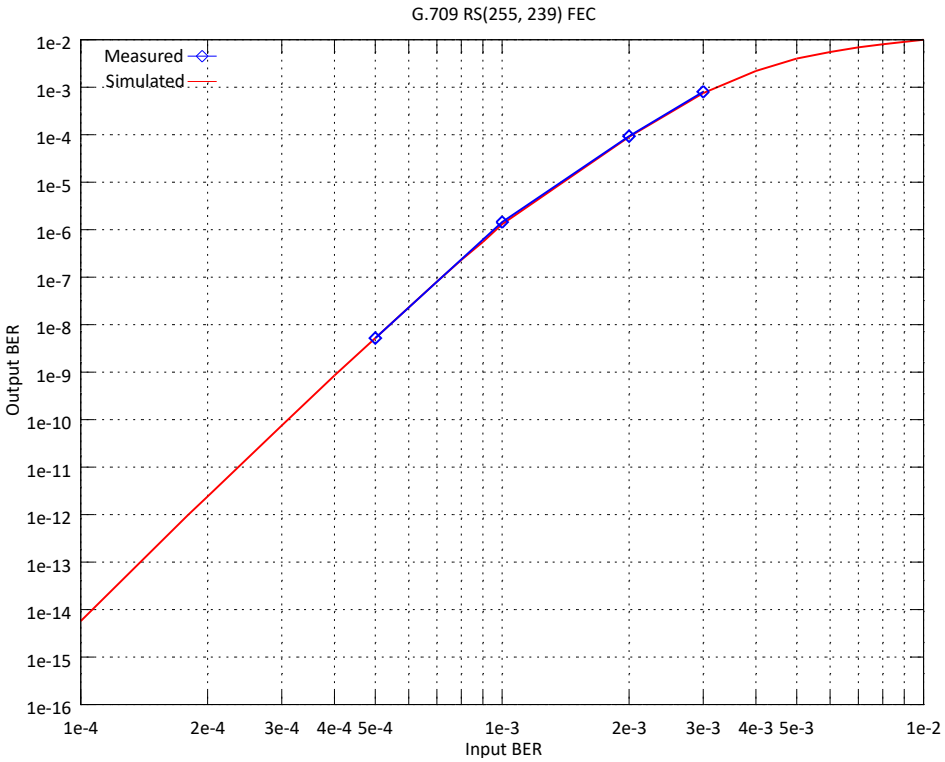

Figure 6. The error-correcting capability of the RS Decoder IP Core RS(255, 239)

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/rs-codec/

Feedback

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Revision history

Version	Date	Changes
3.0	2016.04.05	Improved RS Codec performance.
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.2	2010.12.02	Add WiMAX and WiGig standards support
1.1	2009.09.05	Maintenance improvements
1.0	2007.01.29	Official release