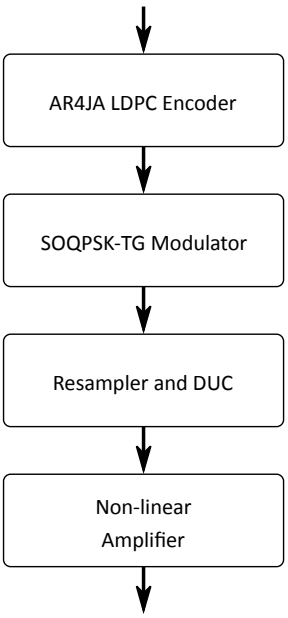
SOQPSK LDPC Modulator IP Core

IP Core Features

- SOQPSK-TG
- AR4JA LDPC FEC
- Variable symbol rate
- Constant envelope signal
- Low FPGA resource usage



Key Features

- Compliant with Telemetry IRIG 106-22 Standard
- Supports SOQPSK-TG, SOQPSK-MIL, SOQPSK-A and SOQPSK-B variants
- Supports all 9 CCSDS AR4JA LDPC encoding schemes:
  - rates 1/2, 2/3. 4/5
  - block sizes 1K, 4K, 16K
- On-the-fly LDPC FEC configuration change
- Symbol rate Fclk/4 to Fclk/65536
- Easy integration with JESD204B DAC

Applications

- Satellite communication systems
- Systems with the need of powerful LDPC Codes
- Power efficient modems with non-linear amplifiers
- Telemetry modems

Deliverables

- Encrypted Netlist or Complete RTL Source Code versions
- IP Core testbench scripts and design examples for evaluation boards
- Comprehensive integration guide
- Free 1 year technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Royalty-free license without quantitative restrictions
- Off-the-shelf Xilinx and Analog Devices evaluation boards support