IPRIUM

Viterbi Decoder IP Core Specification

Information about Release

Product	Viterbi Decoder IP Core
Version	2.1
Build date	2019.04
Ordering Code	ip-viterbi-decoder
Specification revision	r1620

Features

The IP core implements the Viterbi decoding algorithm and is fully compatible with those recommendations:

- Digital Video Broadcasting (DVB-S, DVB-T)
- Intelsat IESS-308/309

The IP Core supports streaming mode only, burst mode is not supported.

Price and License

Price:

- Netlist price : 540 EUR
- Source code price : 7700 EUR
- +10% of the cost for each additional FPGA family netlist
- Customization price is 1000-5000 EUR

License:

- Netlist for One FPGA Family or Full Source Code (Verilog, SDC/XDC)
- Perpetual
- Without Quantitative Restrictions
- Worldwide
- Royalty-free
- Free Remote Technical Support for 1 Year

Deliverables

The Viterbi Decoder IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core structure

Figure 1 shows the Viterbi Decoder IP Core block diagram.

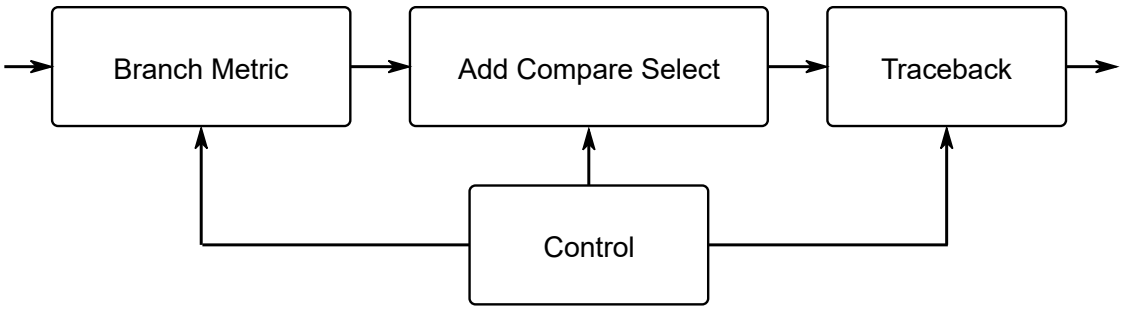

Figure 1. The Viterbi Decoder IP Core block diagram

IP Core has classical structure and contents **Branch Metric**, **Add Compare Select** and **Traceback** blocks. For control and interface purpose there is **Control** block.

Port map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the Viterbi Decoder IP Core.

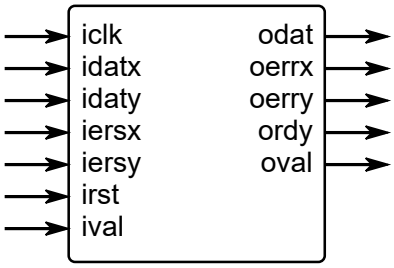

Figure 2. The Viterbi Decoder port map

Table 1. The Viterbi Decoder port map description

Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idatx	W_DAT	input channel data
idaty	W_DAT	input channel data
iersx	1	input data X pattern erase
iersy	1	input data Y pattern erase
irst	1	The IP Core synchronously reset when irst is asserted high.
ival	1	input data valid
odat	1	output decoded data

oerrx	1	corrected error in idatx
oerry	1	corrected error in idaty
ordy	1	ready for new input data
oval	1	output data valid

Soft decision format

Table 2 describes the Viterbi Decoder IP Core input soft decision symbols format.

Table 2. Soft decision symbols format	
011	Strong logical "0"
010	
001	
000	Weak logical "0"
111	Weak logical "1"
110	
101	
100	Strong logical "1"

IP Core parameters

The IP Core uses constraint length **K = 7** and generator polynome **POLY_X_Y = (171, 133) oct.**

Table 3 describes the Viterbi Decoder IP Core parameters, which must be set before synthesis.

Table 3. The Viterbi Decoder IP Core parameters description	
Parameter	Description
W_DAT	input data width, 4
TRB	depth traceback, 42

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 4 summarizes the Viterbi Decoder IP Core measurement results.

Table 4. The Viterbi Decoder performance				
IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_DAT = 4 K = 7 TRB = 42 POLY_X = 171 POLY_Y = 133	Altera Cyclone V 5CEFA7			
	1114 ALMs (1%) 6 M10K RAM blocks (1%) 0 DSP (18x18) (0%)	-8, Fmax	-7, Fmax	-6, Fmax
		135.0 MHz 135.0 Mbit/s	152.0 MHz 152.0 Mbit/s	190.0 MHz 190.0 Mbit/s
W_DAT = 4 K = 7 TRB = 42 POLY_X = 171 POLY_Y = 133	Xilinx Virtex-7 XC7VX330T			
	807 Slices (1%) 5 18K RAM blocks (1%) 0 DSP (18x18) (0%)	-1, Fmax	-2, Fmax	-3, Fmax
		258.0 MHz 258.0 Mbit/s	315.0 MHz 315.0 Mbit/s	350.0 MHz 350.0 Mbit/s

IP Core timing diagrams

Figure 3 shows the Viterbi decoder input timing diagrams. The decoder only accepts data, if "**ordy**" is asserted.

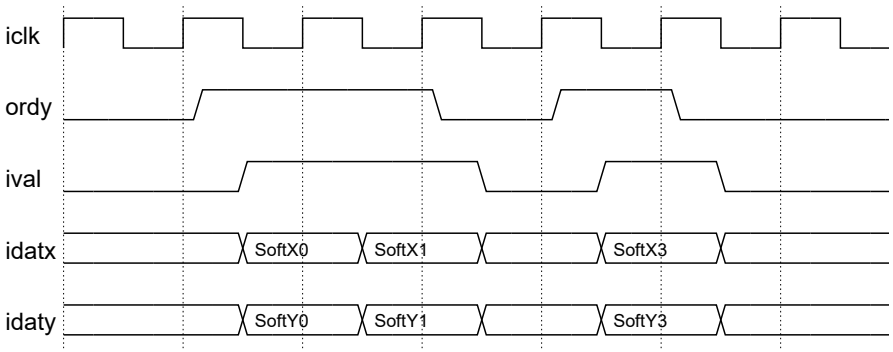

Figure 3. The Viterbi Decoder input timing diagram

Figure 4 shows the Viterbi decoder output timing diagrams. If "**ival**" is continuous, "**oval**" will be continuous. Empty cycles in the input stream will cause empty cycles in the output stream.

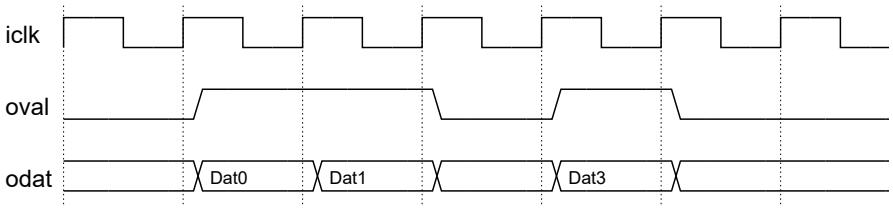

Figure 4. The Viterbi Decoder output timing diagram

Figure 5 shows the Viterbi decoder depuncturing timing diagram and shows "**iersx**", "**iersy**" for the pattern 110110 (pucturing rate 3/4). By changing the "**iersx**", "**iersy**" patterns you can implement virtually any depuncturing pattern you require.

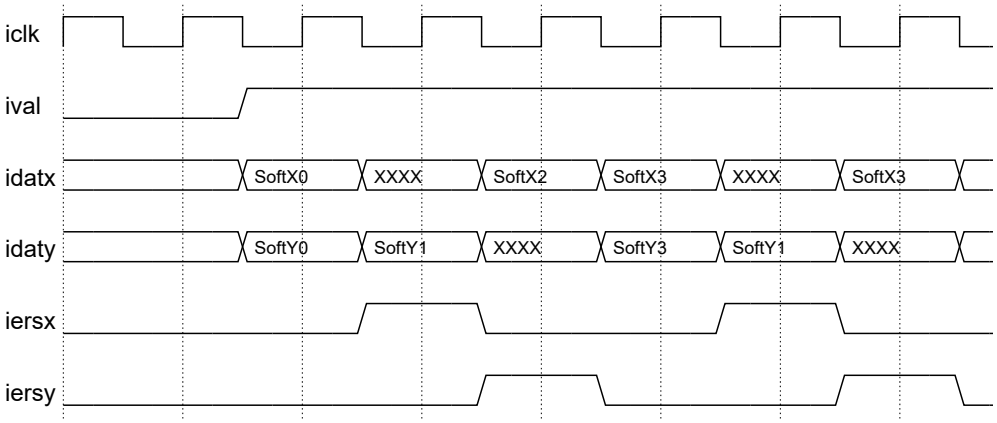

Figure 5. The Viterbi Decoder depuncturing timing diagram

Quality Metrics

The error-correcting capability of the Viterbi Decoder IP Core is shown on the figure 6.

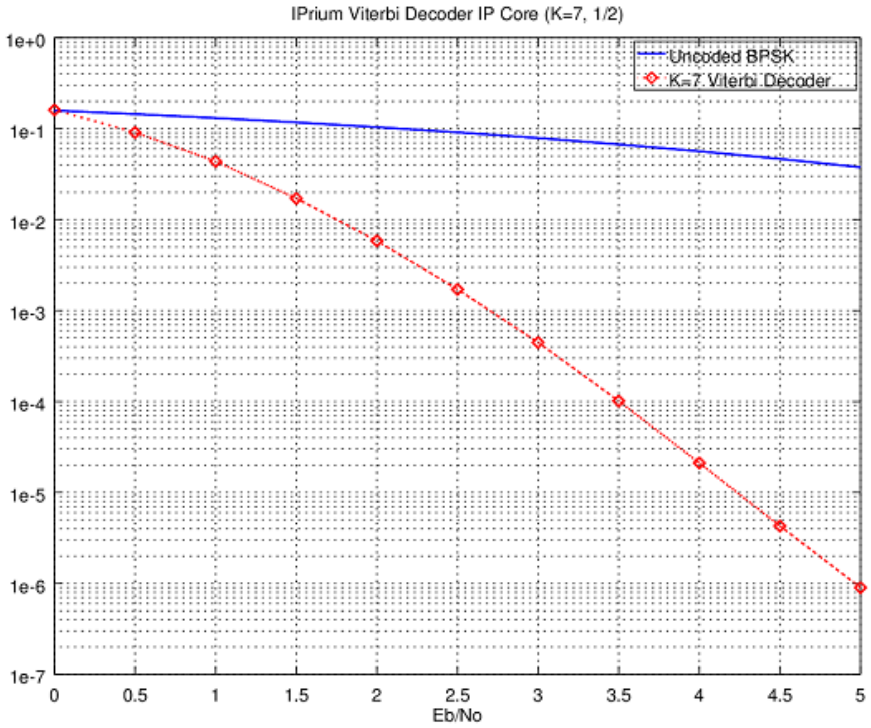

Figure 6. The error-correcting capability of the Viterbi Decoder (K=7, 1/2)

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/viterbi-decoder/

Feedback

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Revision history

Version	Date	Changes
2.1	2019.04.08	Maintenance improvements
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.2	2012.01.10	Changes in control interface
1.1	2009.08.20	Maintenance improvements
1.0	2006.12.06	Official release