Wideband DDC IP Core Specification

Release Information

Name	Wideband DDC IP Core
Version	2.1
Build date	2014.11
Ordering code	ip-wideband-ddc
Specification revision	r1383

Features

The IP core is full-featured wideband digital downconverter and includes complex digital mixer and digital decimation filter with signal gain and phase correction.

Deliverables

The Wideband DDC IP Core includes:

- EDIF/NGC/QXP/VQM netlist for Xilinx Vivado/ISE, Intel (Altera) Quartus, Lattice Diamond or Microsemi (Actel) Libero SoC
- IP Core testbench scripts
- Design examples for Xilinx, Intel (Altera), Lattice, and Microsemi (Actel) evaluation boards

IP Core Structure

Figure 1 shows the Wideband DDC IP Core block diagram.

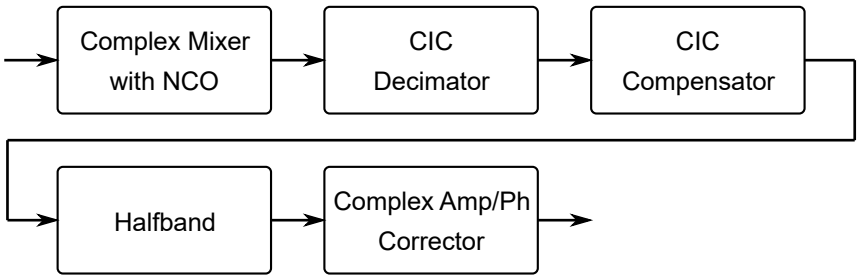

Figure 1. The Wideband DDC IP Core block diagram

Port Map

Figure 2 shows a graphic symbol, and Table 1 describes the ports of the Wideband DDC IP Core.

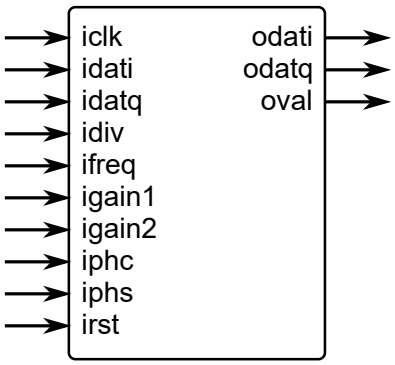

Figure 2. The Wideband DDC port map

Table 1. The Wideband DDC port map description		
Port	Width	Description
iclk	1	The main system clock. The IP Core operates on the rising edge of iclk.
idati idatq	W_ADC*NSPC	Complex IQ input at baseband or at intermediate frequency.
idiv	16	Decimation ratio.
ifreq	32	Input intermediate frequency.
igain1	16	Coarse gain control.
igain2	16	Fine gain control.
iphc iphs	16	Complex input for amplitude and phase correction of the output signal. odat = data * complex(iphc, iphs)
irst	1	The IP Core synchronously reset when irst is asserted high.
odati odatq	W_OUT	Complex IQ output.
oval	1	Output data valid.

IP Core Parameters

Table 2 describes the Wideband DDC IP Core parameters, which must be set before synthesis.

Table 2. The Wideband DDC IP Core parameters description	
Parameter	Description

W_ADC	**ADC Width.** Width of the DDC input samples from ADC (**idati/idatq**).
NSPC	**Number of Samples per Cycle.** Number of parallel ADC samples.
W_OUT	**Output Width.** Width of the DDC output samples (**odati/odatq**).

Performance and Resource Utilization

The values were obtained by automated characterization, using standard tool flow options and the floorplanning script delivered with the IP Core. The IP Core fully supports all Xilinx and Altera FPGA families, including Spartan, Zynq, Artix, Kintex, Virtex, Cyclone, Arria, MAX, Stratix. Table 3 summarizes the Wideband DDC IP Core measurement results.

Table 3. The Wideband DDC performance

IP Core parameters	**FPGA type**			
	Resource	**Speed grade, maximal system frequency**		
W_ADC = 16 NSPC = 8 W_OUT = 25	Altera Cyclone V 5CEFA7			
	9475 ALMs (17%) 88 M10K RAM blocks (13%) 38 DSP (18x18) (25%)	-8, Fmax	-7, Fmax	-6, Fmax
		84.0 MHz 672.0 MSPS	94.0 MHz 752.0 MSPS	111.0 MHz 888.0 MSPS
W_ADC = 16 NSPC = 8 W_OUT = 25	Xilinx Virtex-7 XC7VX330T			
	4258 Slices (9%) 40 18K RAM blocks (3%) 38 DSP (18x18) (4%)	-1, Fmax	-2, Fmax	-3, Fmax
		189.0 MHz 1512.0 MSPS	218.0 MHz 1744.0 MSPS	244.0 MHz 1952.0 MSPS

Quality Metrics

The Wideband DDC IP Core provides the following quality metrics:

- 16 to 65520 decimation ratio in steps 16
- 0.05 dB pass band ripple in 65% bandwidth
- 60 dB stop band rejection
- 70 dB gain range in steps 0.01 dB
- 0.05 degree of phase adjust accuracy
- SFDR 80 dB

Quality metrics of the IP Core can be improved on request.

Upgrade and Technical Support

Free remote technical support is provided for 1 year and includes consultation via phone, E-mail and Skype. The maximum time for processing a request for technical support is 1 business day.

For up-to-date information on the IP Core visit this web page

https://www.iprium.com/ipcores/id/wideband-ddc/

Feedback

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Revision history

Version	Date	Changes
2.1	2014.11.11	Added parallel processing of input complex samples
2.0	2014.09.23	Added support for Xilinx Virtex-7, Kintex-7, Artix-7, Altera Stratix V, Arria V, Cyclone V, Lattice ECP5
1.1	2013.06.13	Added complex signal amplitude and phase correction
1.0	2009.10.20	Official release