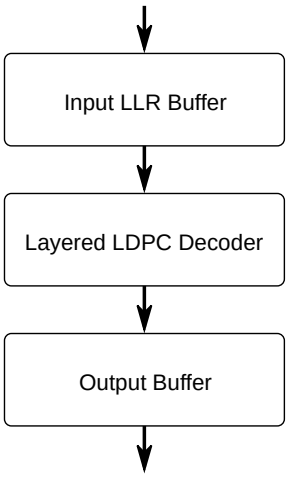
CCSDS 231.0 LDPC Encoder / Decoder IP Core

IP Core Features

- LDPC (128, 64)
- LDPC (512, 256)
- Up to 120 Mbit/s
- Low implementation loss
- Low FPGA resource usage



Key Features

- Compliant with CCSDS 231.0-B-4 Standard, July 2021:
  - TC synchronization and channel coding
- Supports both (128, 64) and (512, 256) LDPC encoding schemes:
  - Encoding rate up to 200 Mbit/s
  - Decoding rate up to 120 Mbit/s
- On-the-fly block type change
- Layered Min-Sum-Offset decoding with low implementation loss
- Decoding early termination mechanism
- Variable number of decoding iterations up to 256

Applications

- Satellite communication systems
- Systems with the need of powerful LDPC Codes
- Telecommand (TC) Space Data Link Protocol modems
- Unified Space Data Link Protocol (USLP) modems

Deliverables

- Encrypted Netlist or Complete RTL Source Code versions
- IP Core testbench scripts and design examples for evaluation boards
- Comprehensive integration guide
- Free 1 year technical support and maintenance updates

Product Options

- IP customization and integration services available on request
- Royalty-free license without quantitative restrictions
- Off-the-shelf Xilinx and Analog Devices evaluation boards support

IPRIUM